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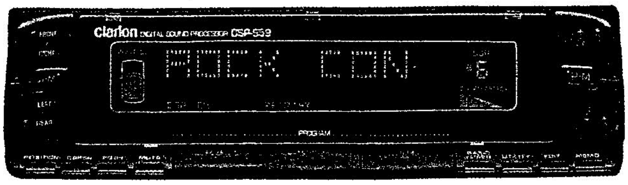
Service Dept.—50 Kamitoda, Toda-shi, Saitama, 335 Japan Tel: 0484-43-1111 Telex: J2962628 CLAFAC-J

clarion Service Manual

Published by Service Administration Section



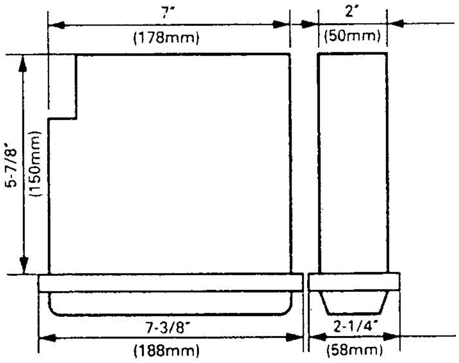
DIGITAL SOUND PROCESSOR

Model DSP-959E (EE-982A-01) (EE-982B-01)

■ SPECIFICATIONS:

Frequency response:	20 Hz to 20 kHz (±0.5dB)
Sampling frequency:	44.1 kHz
S/N Ratio:	Better than 90dB
Channal sepaRation:	Better than 90 dB
THD:	0.02% (1 kHz)
Gain:	0dB
Analog input:	1.5V rms (max.)
Digital input:	44.1 sampling frequency Optical digital audio data
A/D convarsion:	16-bit linear 64 times oversampling
D/A convarsion:	18-bit linear 4 times oversampling
Digital equalizer:	9 frequency bands, 8 EQ curve memories (4 pri-programmed/4 user-programmed)
Center frequencies:	63 Hz, 125 Hz, 250 Hz, 500 Hz, 1 kHz, 2 kHz, 4 kHz, 8 kHz, 16 kHz

Digital sound field:	16 memories (8 user-programmed)
Memory:	256 kBit ×2 (PS-RAM)
Power requirements:	14.4V negative ground
Power consumption:	800 mA
Wait:	1.1 kg
Dimensions:	



* Design and specifications are subject to change without notice for improvements.

■ COMPONENTS:

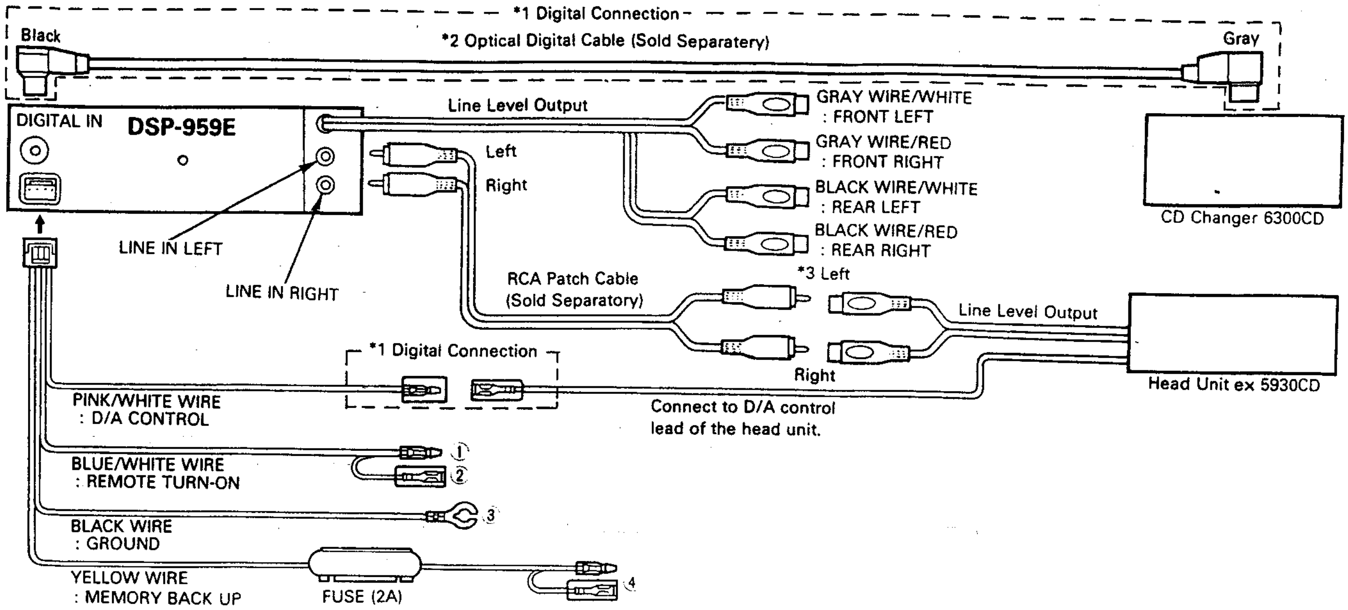
◎ EE-982A-01

Main unit		1
Owners manual	280-5820-00	1
Warranty card		1
Power cord ass'y	653-0197-01	1
Mounting blacked	300-4976-00	1
Silicagel	258-0023-00	1
Part bag	921-8673-00	1
Hook plate	330-8216-01	(2)
tapping screw 5x16	700-5016-80	(1)
Machine screw	714-5008-41	(4)
Screw	716-0496-01	(5)
Screw	716-0726-01	(1)
Nut	722-0314-00	(1)
Plate nut	725-0216-00	(1)
Face bag	922-2153-00	1
Mounting blacket	300-9035-01	1

◎ EE-982B-01

Main unit		1
Owners manual	280-5821-00	1
Warranty card		1
Power cord ass'y	653-0197-01	1
Mounting blacked	300-6954-00	1
Silicagel	258-0023-00	1
ISO 10 cord ass'y	854-2609-00	1
Part bag	921-8740-00	1
Hook plate	330-8216-01	(2)
Spacer	345-3653-01	(1)
tapping screw 5x16	700-5016-80	(1)
Screw	716-0496-01	(1)
Screw	716-0726-01	(1)
Nut	722-0314-00	(1)
Plate nut	725-0216-00	(1)
Face bag	922-2153-00	1
Mounting blacket	300-9035-01	1

■WIRE CONNECTION:


*1 Digital Connection
Black
*2 Optical Digital Cable (Sold Separatery)
Gray
DIGITAL IN
DSP-959E
Line Level Output
GRAY WIRE/WHITE
: FRONT LEFT
GRAY WIRE/RED
: FRONT RIGHT
BLACK WIRE/WHITE
: REAR LEFT
BLACK WIRE/RED
: REAR RIGHT
Left
Right
CD Changer 6300CD
LINE IN LEFT
LINE IN RIGHT
RCA Patch Cable
(Sold Separatory)
*3 Left
Line Level Output
Right
Head Unit ex 5930CD
*1 Digital Connection
PINK/WHITE WIRE
: D/A CONTROL
Connect to D/A control
lead of the head unit.
BLUE/WHITE WIRE
: REMOTE TURN-ON
①
②
BLACK WIRE
: GROUND
③
YELLOW WIRE
: MEMORY BACK UP
FUSE (2A)
④

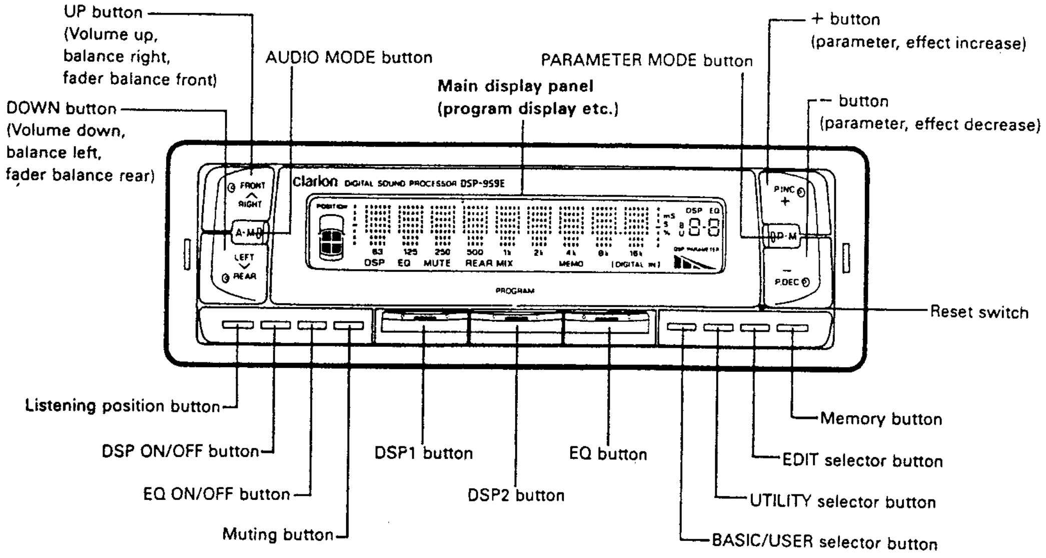
*1. D/A CONTROL LEAD (pink/white wire)
Connect to D/A Control Lead of head unit to select Digital or Analog connection automatically in case both the Digital and Analog connections are made.
DO NOT connect any lead to this lead in case you do not make the digital connection.

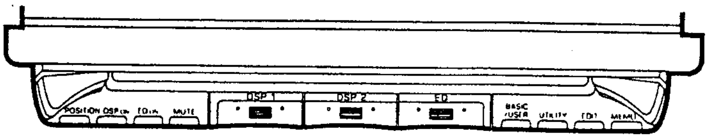
*2. OPTICAL DIGITAL CABLE (sold separately)
DCA-001-100 16 feet
DCA-002-100 5 feet

*3. Analog Line Level Input
Connect to either Front or Rear Line Level Output of your head unit.

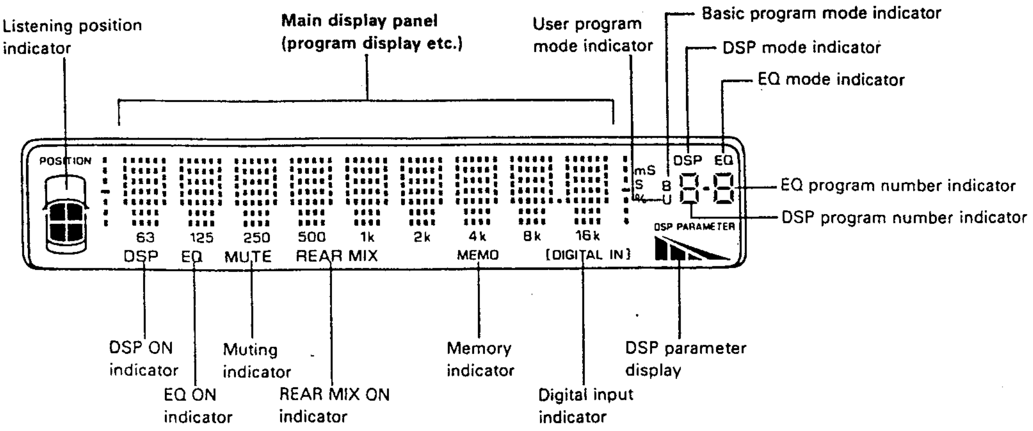
CONTROL POSITION OF HEAD UNIT.
Volume: Maximum level
Bass/Treble/Balance/Fader: Center positions
Mute/Loudness: OFF

① Connect to remote switching lead or power antenna lead of head unit.
② Connect to power antenna activator lead or the remote switching lead of the power amplifier (max. 0.5A current drain).
③ Connect to vehicle sheet metal.
Scrape paint to assure good contact.
④ Connect to +12V continuous (unswitched) power source.


UP button
(Volume up,
balance right,
fader balance front)
DOWN button
(Volume down,
balance left,
fader balance rear)
AUDIO MODE button
Main display panel
(program display etc.)
PARAMETER MODE button
+ button
(parameter, effect increase)
– button
(parameter, effect decrease)
Clarion DIGITAL SOUND PROCESSOR DSP-959E
FRONT
RIGHT
A-M
LEFT
REAR
P-INC
+
P-M
–
P-DEC
POSITION
63 125 250 500 1k 2k 4k 8k 16k
DSP EQ MUTE REAR MIX MEMO (DIGITAL IN)
PROGRAM
Reset switch
Listening position button
DSP ON/OFF button
EQ ON/OFF button
Muting button
DSP1 button
DSP2 button
EQ button
Memory button
EDIT selector button
UTILITY selector button
BASIC/USER selector button

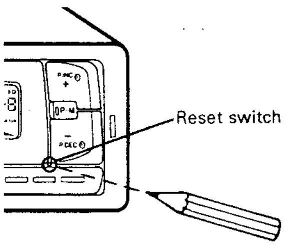

POSITION DSP ON EQ ON MUTE
DSP 1
DSP 2
EQ
BASIC /USER UTILITY EDIT MEMORY

■ DISPLAY PANEL


Listening position indicator
Main display panel (program display etc.)
User program mode indicator
Basic program mode indicator
DSP mode indicator
EQ mode indicator
POSITION
63
125
250
500
1k
2k
4k
8k
16k
mS
S
B
DSP
EQ
DSP PARAMETER
DSP
EQ
MUTE
REAR MIX
MEMO
[DIGITAL IN]
EQ program number indicator
DSP program number indicator
DSP ON indicator
EQ ON indicator
Muting indicator
REAR MIX ON indicator
Memory indicator
Digital input indicator
DSP parameter display

If trouble has occurred, such as if the unit does not operate when an operation button is pressed or the display does not display the proper information, press the Reset button for about 2 seconds with a pencil or another sharp object and then use the unit as normal.

CAUTION: Pressing the Reset button will erase all information stored in memory.


Reset switch

■FEATURES:

- ■Digitally Recreates Different Sound Field environments
- ■8 Pre-programmed/8 User Programable Sound Field Memories
- ■Digital 9 Band Graphic E.Q. w/4 Pré-programmed and 4 User Programmable E.Q. Curve Memories
- ■5 Presets for Seating Positions
- ■3 Presets for Different Interior Size
- ■Built in Pink Noise Generator
- ■Digital Fiber Optic Input
- ■Button Illumination with Dual Color Selector
- ■Adjustable Gain for Direct Sound Rear Channel Output
- ■Gold Plated RCA Connectors

■ADJUSTMENT:

The main sheet Ass'y VR-601 is adjusted so as both ends of C660 (or between GND of To DSP [1] and +5V) become $5^{+0.2}_{-0.1}$ V.

o Test Program

This test program is a checkup software which is set up for performing speedy functional operations at production factories and marketing services.

Cautions

* Because memories are initialised when the test program is executed, user set-up parameter values are also cleared.

* Because it is in the initial state VOL MAX when the test program is executed, speakers are likely to be damaged if it is executed when the sound of the Head Unit is generated.

① How to start up

Press the key $\boxed{\text{memo}}$ after the power is ON. Then press the key $\boxed{\text{amode}}$ within 5 secs.

The system starts up if $\boxed{\text{reset}}$ is pressed within 10 secs.

② Self diagnosis

The test program performs error checking, and if there is any error, the error is displayed for 5 seconds. Also, if error occurs, the buzzer flag is cleared so that there will be no buzzer from then on.

Error display and contents of checkup are indicated below. It is confirmed if the system software is working properly and if the operations are performed properly in accordance with the software by these checkups.

Error Display	Contents of checkup	
ERROR 1	ROM quality judgement	Contents of ROM write check
ERROR 2	CPU internal RAM quality judgement	WRITE, READ check
ERROR 3	Externally attached RAM quality judgement	WRITE, READ check
ERROR 5	DEQ, DSP transmission quality judgement	

Letters V ☐☐ are displayed after version display error is checked up.

The ROM version is found by this. ☐☐ part of V ☐☐ is modified when the ROM software is changed.

③ Test mode menu

The test mode consists of the following menu:

a. LCD check

b. LED check

c-1. RAM through

c-2. DSP through

d. EQ check

e. VOL UP/DOWN

f. MUTE ON/OFF

g. Buzzer check

The initial states are:

LCD display (RAM)
LED (GREEN)
Signal is RAM through
EQ is flat
VOL is MAX.
MUTE is OFF
BAL/FAD is center

a. LCD check

LCD is lit when POSITION is pressed after starting the test program.

From then on, pressing the key POSITION repeats the entire lights off and the entire lights on.

b. LED check

The LED color is switched when the key BASIC/USER is pressed.

(Amber ↔ Green)

c. Signal check

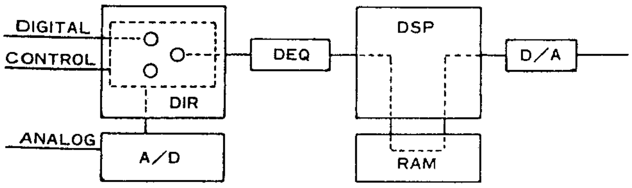
When EQ is flat, BAL/FAD is center and VOL is 39, it is possible to switch between digital and analog by the entire channels 0dB or by external control terminals.

RAM through

RAM is displayed when the test program starts up, and the signal becomes RAM through.

From then on, DSP through and RAM through is switched over when the key DSP ON is pressed.

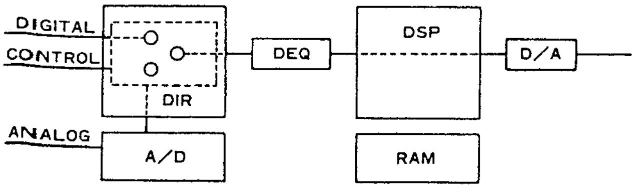
There is a delay of approximately 186 ms in RAM through.



DSP through

In RAM through, DSP is displayed when the key DSP ON is pressed, and the signal becomes DSP through.

From then on, DSP through and RAM through is switched over when the key DSP ON is pressed.



d. EQ check

It becomes DSP through and the 1 kHz EQ measurement mode when the key EQ ON is pressed.

The gain of blinking frequency becomes +12dB by the parameter UP key, and becomes -12dB by the DOWN key.

If the frequency is shifted one to the right by the key P.MODE , also the entire bands becomes flat.

e. VOL UP/DOWN

In the test program, it is MAX (39) on start up.

It is changed by the key UP/DOWN .

f. MUTE ON/OFF

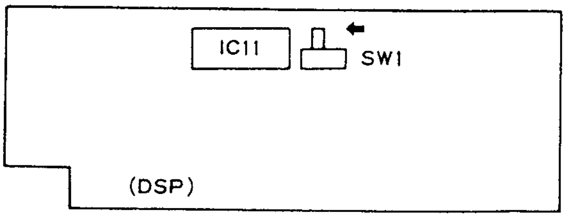
It becomes 20dB by the key MUTE . During MUTE ON, the MUTE display is blinking.

g. Buzzer check

The buzzer keeps on buzzing while the key EDIT is being pressed.

④ How to end the test program

When ending the test program, either the key RESET is pressed or the REMOTE terminal of AMP is ON/OFF.



o SW1 for service

This system possesses SW1 as a service.

When SW1 is made to the right (opposite ICII) as shown in the figure below, it is possible to jump DSP and DEQ circuits to output so that when failure occurs, it facilitates to identify whether the failure comes from DSP, DEQ circuits (including IC) or something other than those.

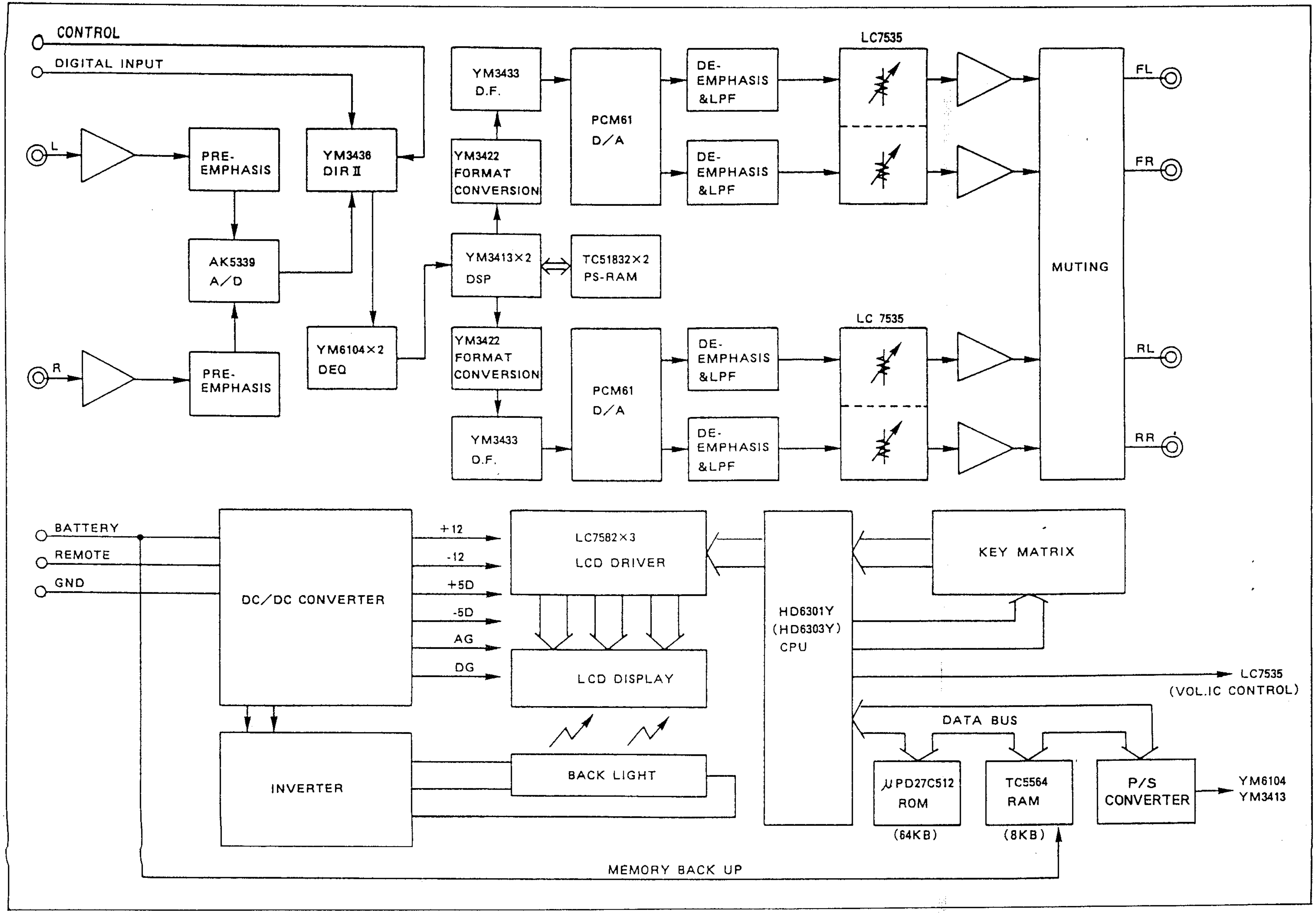
Normally, it is levelled at the direction where ← is indicated (ICII side) as shown in the figure below.

o "Digital in" display on RESET operation

If the RESET operation is performed when the power of this system is ON, "Digital in" may be displayed for approximately 0.5 secs.

Note) This occurs as the FSI terminal of DIR-II (IC24) which is connected to the microcomputer (IC312) on P64 is an input dependent type indeterminate port, a flag may be on for FS1 when power is ON, so that the microcomputer detects it on RESET operation and "Digital in" is displayed instantaneously, which is usually irrelevant to operations. It is the operation limited to the RESET operation only.

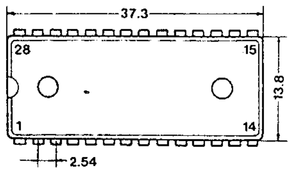
■BLOCK DIAGRAM:


CONTROL
DIGITAL INPUT
L
R
PRE-EMPHASIS
PRE-EMPHASIS
AK5339 A/D
YM3436 DIR II
YM6104×2 DEQ
YM3433 D.F.
YM3422 FORMAT CONVERSION
YM3413×2 DSP
TC51832×2 PS-RAM
YM3422 FORMAT CONVERSION
YM3433 D.F.
PCM61 D/A
PCM61 D/A
DE-EMPHASIS &LPF
DE-EMPHASIS &LPF
DE-EMPHASIS &LPF
DE-EMPHASIS &LPF
LC7535
LC 7535
MUTING
FL
FR
RL
RR
BATTERY
REMOTE
GND
DC/DC CONVERTER
+12
-12
+5D
-5D
AG
DG
LC7582×3 LCD DRIVER
LCD DISPLAY
BACK LIGHT
INVERTER
HD6301Y (HD6303Y) CPU
KEY MATRIX
LC7535 (VOL.IC CONTROL)
DATA BUS
μPD27C512 ROM (64KB)
TC5564 RAM (8KB)
P/S CONVERTER
YM6104
YM3413
MEMORY BACK UP

■EXPLANATION OF MAIN IC's:

■AK5339-VP 653-0198-74 16-bits ΔΣ mode 2-channel A/D Converter

Outward Form

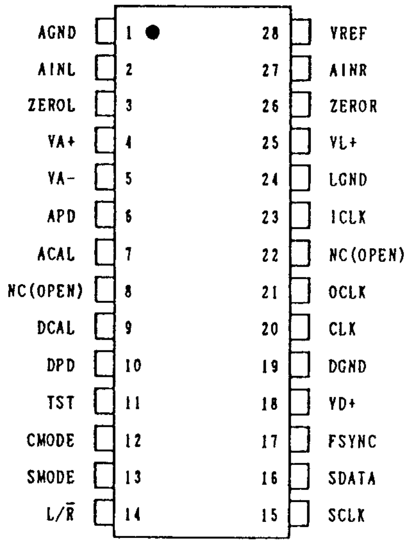

37.3
28
15
1
14
13.8
2.54

General

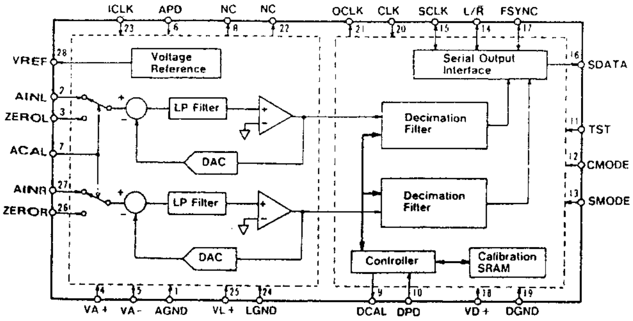
This IC is a 16-bit 2-channel A/D converter utilizing the four-dimensional mode. Two built-in ΔΣ modulators sample analog input signals simultaneously at 64-fold sampling rate (64 fs). Over-sampled data is decimated to 16-bit data of fs through the digital filter.

The built-in reference voltage source provides voltage input of ±3.68V. Offset error is canceled by starting the calibration cycle when power is turned on. The calibration cycle may be started at any time. Output data consists of 16-bit serial data coded with 2's compliment and 3-bit OVER/UNDER scale flag and L/R flag.

Terminal Connection


AGND 1
AINL 2
ZEROL 3
VA+ 4
VA- 5
APD 6
ACAL 7
NC(OPEN) 8
DCAL 9
DPD 10
TST 11
CMODE 12
SMODE 13
L/$\overline{R}$ 14
28 VREF
27 AINR
26 ZEROR
25 VL+
24 LGND
23 ICLK
22 NC(OPEN)
21 OCLK
20 CLK
19 DGND
18 VD+
17 FSYNC
16 SDATA
15 SCLK

Block Diagram


ICLK
APD
NC
NC
OCLK
CLK
SCLK
L/$\overline{R}$
FSYNC
VREF
AINL
ZEROL
ACAL
AINR
ZEROR
Voltage Reference
LP Filter
DAC
LP Filter
DAC
Serial Output Interface
Decimation Filter
Decimation Filter
Controller
Calibration SRAM
SDATA
TST
CMODE
SMODE
VA+
VA-
AGND
VL+
LGND
DCAL
DPD
VD+
DGND

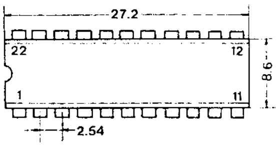
Terminal Description

Pin No.	Symbol	I/O	Function
1	AGND	–	Analog ground terminal in analog unit.
2	AINL	I	Lch analog input terminal.
3	ZEROL	I	Lch zero level input terminal. Normally, offset of Lch is calibrated with input voltage at this terminal as zero. The terminal is connected to AGND terminal.
4	VA+	–	Analog positive power terminal in analog unit (+5V).
5	VA–	–	Analog negative power terminal in analog unit (–5V).
6	APD	I	Power-down terminal in analog unit. When this terminal is turned to "H", the analog unit is put in the POWER-DOWN mode.
7	ACAL	I	Analog calibration terminal. Normally, the terminal is connected to DCAL terminal. External signal input terminal is selected according to the level of the terminal. "H" : Zero level input terminal (ZEROL, ZEROR) "L" : Analog input terminal (AINL, AINR)
8	NC	–	Not connected (open).
9	DCAL	O	Digital calibration terminal indicating execution of the offset calibration. Normally, the terminal is connected to ACAL terminal. When POWER-DOWN signal is received by DPD terminal, this terminal is turned to H. After 4096L/$\overline{R}$ cycles (about 85ms with fs=48kHz) following turn-off of the DPD terminal, the terminal is turned to "L" to indicate the end of calibration.
10	DPD	I	POWER-DOWN terminal in digital unit. When the terminal is turned to "H", the digital unit is put in the POWER-DOWN mode. When it is turned to "L", offset calibration starts.
11	TST	I	Test terminal connected to DGND terminal.
12	CMODE	I	A terminal used to select master clock. "L" : CLK=256fs (12.288MHz @fs=48kHz) "H" : CLK=384fs (18.432MHz @fs=48kHz)
13	SMODE	I	A terminal used to select I/O of interface clocks L/$\overline{R}$, SCLK and FSYNC. "L" : Slave mode (all terminals act as input terminals) "H" : Master mode (all terminals act as output terminals)
14	L/$\overline{R}$	I/O	A terminal used to select input channel. Slave mode: The terminal receives fs clocks. At its leading edge, MSB data of Lch is sent and MSB data of Rch is sent at the falling edge. Master mode: The terminals sends fs clocks. Data is sent 1 SCLK later following the edge of L/$\overline{R}$. The terminal is turned to "H" when power is turned off (with DPD turned to "H").
15	SCLK	I/O	Serial data clock terminal. When the terminal is turned off, output data is sent by 1 bit. Slave mode: The terminal receives clock of 32 to 64fs. Master mode: The terminal sends clock of 64fs. The terminal is turned to "L" when power is turned off (with DPD turned to "H").
16	SDATA	O	Serial data output terminal. Data is sent from MSB at the compliment of 2's one by one. After sending 16-bit of data, 3-bit OVER/UNDER SCALE flag and L/$\overline{R}$ flag are sent. The terminal is turned to "L" when power is turned off (with DPD turned to "H").
17	FSYNC	I/O	Frame synchronizing clock terminal. Slave mode: When the terminal is turned to "H", output of SDATA is enabled. Master mode: The terminal sends clock of 2fs. When sending 16-bit data, the terminal is turned to "H" to latch data. The terminal is turned to "L" when power is turned off (with DPD turned to "H").
18	VD+	–	Power terminal for digital unit (+5V).
19	DGND	–	Ground terminal for digital unit.

Pin No.	Symbol	I/O	Function
20	CLK	I	Master clock input terminal. CMODE="H" : 384fs CMODE="L" : 256fs
21	OCLK	O	128fs clock output terminal. The terminal toggles at the leading edge of master clock (CLK). When power is turned off (with DPD turned to "H"), the terminal is turned to "L".
22	NC	–	Not connected (open).
23	ICLK	I	128fs clock input terminal. Clock of analog unit. The terminal is connected to OCLK terminal. Sampling rate of $\Delta\Sigma$ modulator is 64fs.
24	LGND	–	Logic ground terminal for analog unit.
25	VL+	–	Logic power terminal for analog unit (+5V).
26	ZEROR	I	Rch zero level input terminal. Normally, Rch offset is calibrated with input voltage of this terminal as zero. The terminal is connected to AGND terminal.
27	AINR	I	Rch analog input terminal.
28	VREF	O	Reference voltage output terminal (−3.68V). Full scale of input signal depends on this voltage. When VREF=−3.68V, FS=±3.68V.

■LC7535 653-0198-15 High Voltage Withstand Serial Control Electronic Volume

Outward Form


27.2
22
12
8.6
1
11
2.54

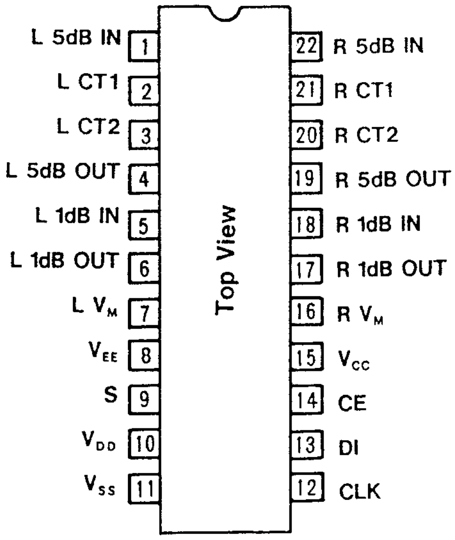
Outline

This IC is an electronic volume which electronically controls volume, balance and loudness functions with a few external parts.

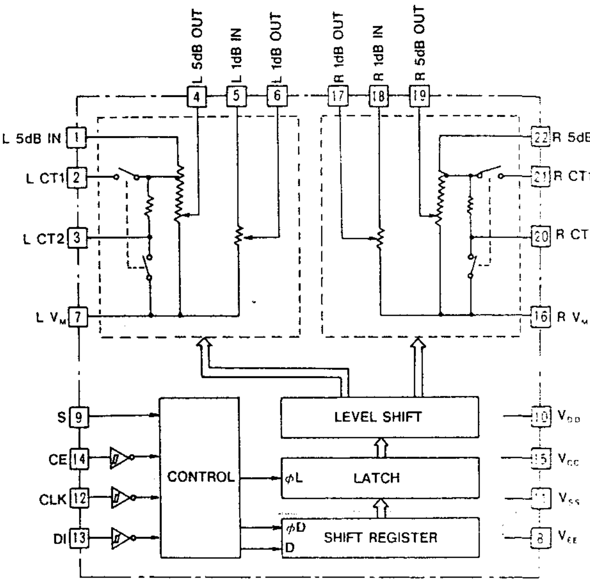
Features

- S (select) terminal which controls with three-line serial data (DI, CLK and CE) common to other ICs enables use of up to two ICs in a same three-line path.
- 1dB step, 80 positions + (−∞) and max. reduction higher than 80dB.
- Input impedance (5dB input): 47kΩ (typ).
- High voltage withstand: ±16V
- Loudness can be controlled by an external capacitor through a center tap provided from the position of −20dB.

Terminal Connection

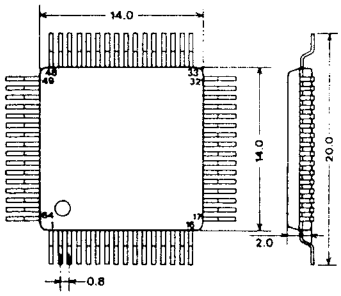

L 5dB IN 1
L CT1 2
L CT2 3
L 5dB OUT 4
L 1dB IN 5
L 1dB OUT 6
L VM 7
VEE 8
S 9
VDD 10
VSS 11
22 R 5dB IN
21 R CT1
20 R CT2
19 R 5dB OUT
18 R 1dB IN
17 R 1dB OUT
16 R VM
15 VCC
14 CE
13 DI
12 CLK
Top View

Block Diagram


L 5dB OUT
L 1dB IN
L 1dB OUT
R 1dB OUT
R 1dB IN
R 5dB OUT
4
5
6
17
18
19
L 5dB IN 1
L CT1 2
L CT2 3
L VM 7
22 R 5dB IN
21 R CT1
20 R CT2
16 R VM
S 9
CE 14
CLK 12
DI 13
CONTROL
LEVEL SHIFT
φL
LATCH
φD
D
SHIFT REGISTER
10 VDD
15 VCC
11 VSS
8 VEE

■LC7582 051-0836-00 Driver For LCD-Display

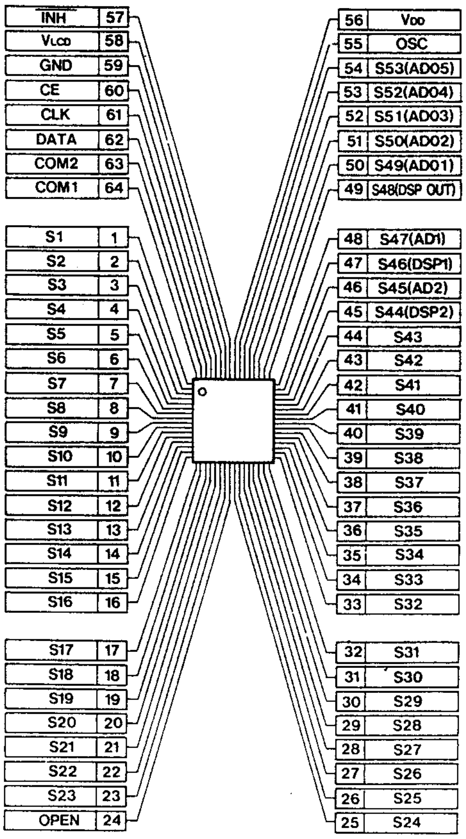
Outward Form


14.0
48
49
33
32
64
1
17
16
14.0
20.0
2.0
0.8

Features

- ● LC7582 is LCD-driver by micro-computer control or frequency display of electronic tuning.
- ● Driving system is made up of 1/1 duty (53 segments) and 1/2 duty (104 segments).
- ● Data input is made with serial-in 3 pcs.
- ● 5-level AD-converter is provided with 2 terminals.
  (as with level-meter use)
- ● Display for direct expression (DSP) with 2 terminals.
- ● With $\overline{\text{INH}}$ terminal for putting out the display.

Terminal Connection



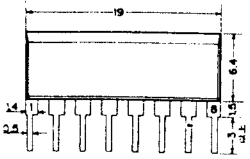
INH 57
VLCD 58
GND 59
CE 60
CLK 61
DATA 62
COM2 63
COM1 64
S1 1
S2 2
S3 3
S4 4
S5 5
S6 6
S7 7
S8 8
S9 9
S10 10
S11 11
S12 12
S13 13
S14 14
S15 15
S16 16
S17 17
S18 18
S19 19
S20 20
S21 21
S22 22
S23 23
OPEN 24
56 VDD
55 OSC
54 S53(AD05)
53 S52(AD04)
52 S51(AD03)
51 S50(AD02)
50 S49(AD01)
49 S48(DSP OUT)
48 S47(AD1)
47 S46(DSP1)
46 S45(AD2)
45 S44(DSP2)
44 S43
43 S42
42 S41
41 S40
40 S39
39 S38
38 S37
37 S36
36 S35
35 S34
34 S33
33 S32
32 S31
31 S30
30 S29
29 S28
28 S27
27 S26
26 S25
25 S24

Terminal Function Table

Pin No.	Terminal Name	Function
1 - 23	S1 · S23	Segment output terminal.
25 - 44	S24 · S43	
24	OPEN	NC
45	S44(DSP2)	Segment output or DSP input.
47	S46(DSP1)	
46	S45(AD2)	Segment output or AD input.
48	S47(AD7)	
49	S48(DSP OUT)	Segment output or DSP output.
50 ⅰ 54	S49(AD 01) ⅰ S53(AD 05)	Segment output or AD output.
55	OSC	Oscillation terminal.
56	V_{DD}	Power supply terminal.
57	$\overline{\text{INH}}$	Display-putting off input terminal (It is effective for output driver alone, thus it is possible to transfer the serial data during the putting-out of lamp).
58	V_{LCD}	LCD Bias voltage terminal.
59	GND	Ground.
60	CE	Input terminal for transferring the serial data.
61	CLK	
62	DATA	
63	COM2	Common output terminal. (Using COM1 alone at time of 1/1 duty)
64	COM1	

■M62021L 653-0197-94 System Reset IC with Built-in Memory Backup Select Switch

Outward Form



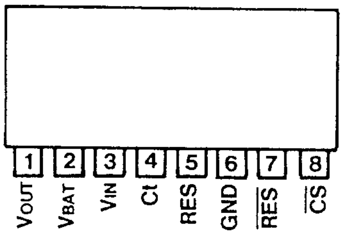
19
6.4
1.4
2.5
1
8
1.5
3

Outline

This IC is a system reset IC which controls memory backup functions of SRAM and microprocessor (with built-in RAM).

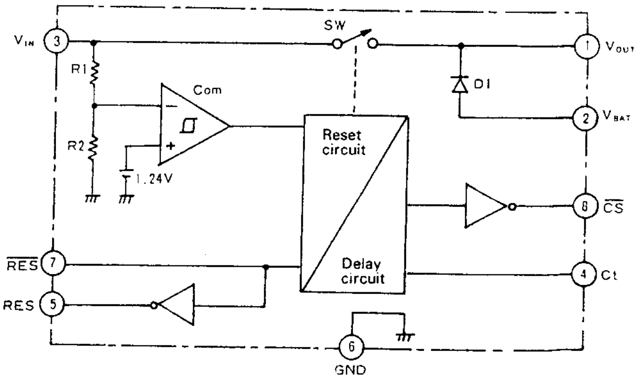
When power is turned on or power fault occurs, the IC sends RESET signal (RES·$\overline{\text{RES}}$) to the microprocessor. Simultaneously, it changes power supply of RAM from the main power supply to the backup power supply and sends STANDBY signal ($\overline{\text{CS}}$) to turn RAM to the backup circuit.

Terminal Connection



1 VOUT
2 VBAT
3 VIN
4 Ct
5 RES
6 GND
7 RES
8 CS

Block Diagram



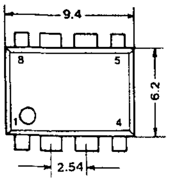
VIN 3
R1
R2
Com
1.24V
SW
D1
Reset circuit
Delay circuit
1 VOUT
2 VBAT
8 CS
4 Ct
RES 7
RES 5
6 GND

Terminal Description

Pin No.	Symbol	Terminal	Function
1	V_{OUT}	POWER OUTPUT	A terminal which controls V_{IN} and V_{BAT} with internal switch to provide V_{OUT}.
2	V_{BAT}	BACKUP POWER INPUT	A terminal which connects backup power supply.
3	V_{IN}	POWER INPUT	+5V input terminal which connects logic power supply.
4	C_t	DELAY CAPACITY ADDITIVE	A terminal which connects delay capacity. Respective outputs can be delayed by connecting capacity.
5	RES	POSITIVE RESET OUTPUT	A terminal which connects the IC to positive reset input of the microprocessor.
6	GND	GROUND	A terminal which provides reference signal.
7	$\overline{\text{RES}}$	NEGATIVE RESET OUTPUT	A terminal which connects the IC to negative reset input of the microprocessor.
8	$\overline{\text{CS}}$	CHIP SELECT OUTPUT	A terminal which connects the IC to CHIP SELECT INPUT of RAM. Normally, CS output is turned to Low to make RAM active. When a fault occurs or memory is backupped, the terminal is turned to High, placing RAM in the STANDBY mode in which writing and reading of RAM is disabled.

■MB3776A 653-0197-95 Switching Regulator Controller

Outward Form

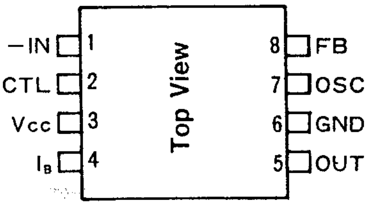

9.4
8
5
1
4
6.2
2.54

Outline

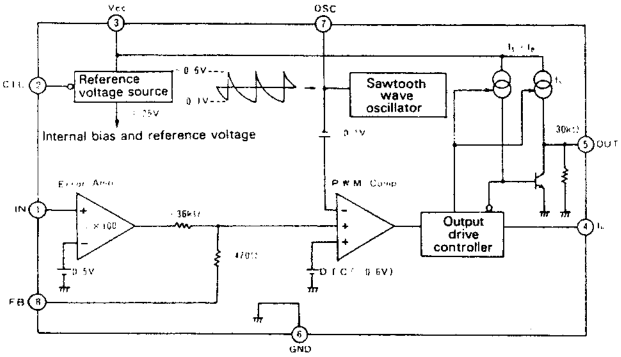
This IC is a PWM type switching regulator controller.

- ○Gain is fixed.
- ○Compatible with low-voltage operation.
- ○Power ON/OFF control is incorporated.

Terminal Connection

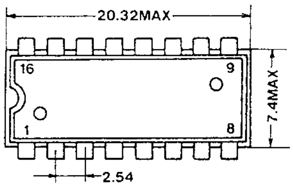

−IN 1
CTL 2
Vcc 3
I_B 4
Top View
8 FB
7 OSC
6 GND
5 OUT

Block Diagram

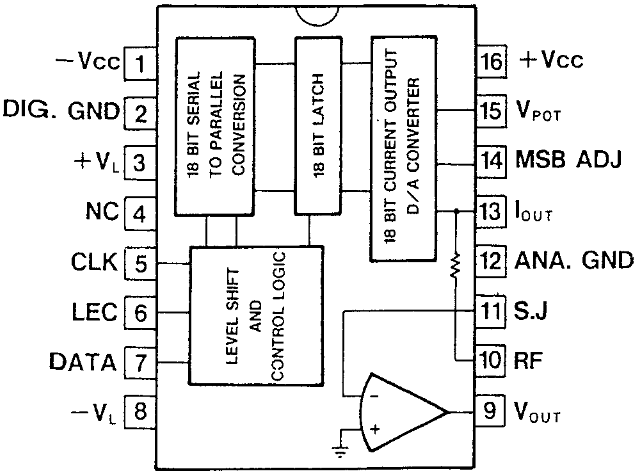

Vcc 3
OSC 7
CTL 2
Reference voltage source
0.6V
0.1V
Sawtooth wave oscillator
I₁ + I₂
I₁
Internal bias and reference voltage
30kΩ
5 OUT
Error Amp
PWM Comp
IN 1
×100
36kΩ
470Ω
0.5V
DTC (0.6V)
Output drive controller
4 I₁
FB 8
6 GND

■PCM61P 653-0198-73 18-bit Serial Input D/A Converter

Outward Form


20.32MAX
16
9
1
8
7.4MAX
2.54

Block Diagram

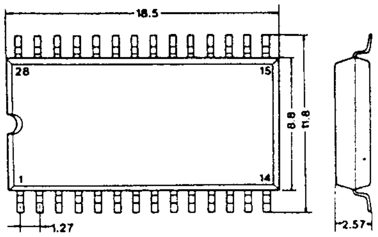

−Vcc 1
DIG. GND 2
+V_L 3
NC 4
CLK 5
LEC 6
DATA 7
−V_L 8
18 BIT SERIAL TO PARALLEL CONVERSION
18 BIT LATCH
18 BIT CURRENT OUTPUT D/A CONVERTER
LEVEL SHIFT AND CONTROL LOGIC
16 +Vcc
15 V_POT
14 MSB ADJ
13 I_OUT
12 ANA. GND
11 S.J
10 RF
9 V_OUT

Terminal Description

Pin No.	Symbol	Function
1	−Vcc	Negative analog power
2	DIG. GND	Digital ground
3	$+V_L$	Positive logic power
4	NC	Not connected
5	CLK	Clock input
6	LEC	Latch enable input
7	DATA	Serial data input
8	$-V_L$	Negative logic power
9	V_{OUT}	Voltage output
10	RF	Feedback resistance
11	S.J	Summing junction
12	ANA. GND	Analog ground
13	I_{OUT}	Current output
14	MSB ADJ	MSB adjustment terminal
15	V_{POT}	MSB trim potentiometer terminal
16	+Vcc	Positive analog power

■TC51832FL-10 653-0198-72 32768 Words×8-Bits CMOS Dummy Static RAM

Outward Form


18.5
28
15
1
14
8.8
11.8
1.27
2.57

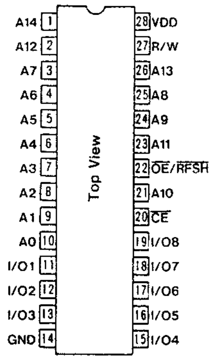
Outline

This IC is a dummy static RAM of 32768 words × 8 bits configuration driven by a single 5V power supply.

Access Time

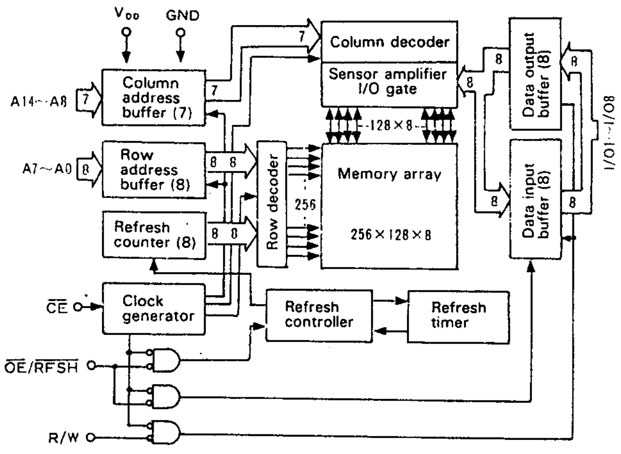
- ○t_{CEA} $\overline{CE}$ access time : 100ns
- ○t_{OEA} $\overline{OE}$ access time : 40ns
- ○t_{RC} cycle time : 160ns

Terminal Connection


A14 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
I/O1 11
I/O2 12
I/O3 13
GND 14
Top View
28 VDD
27 R/W
26 A13
25 A8
24 A9
23 A11
22 OE/RFSH
21 A10
20 CE
19 I/O8
18 I/O7
17 I/O6
16 I/O5
15 I/O4

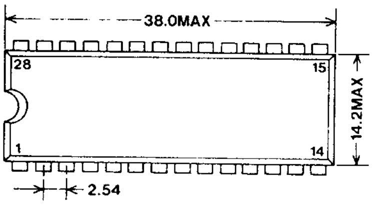
A0~A14	Address Input
R/W	Read/Write Input
$\overline{OE}/\overline{RFSH}$	Output Enable Input/Refresh Input
$\overline{CE}$	Chip Enable Input
I/O1~I/O8	Data I/O
V_{DD}	Power Terminal
GND	Ground

Block Diagram


VDD
GND
A14~A8
7
Column address buffer (7)
A7~A0
8
Row address buffer (8)
Refresh counter (8)
CE
Clock generator
OE/RFSH
R/W
Column decoder
Sensor amplifier I/O gate
128×8
Memory array
256×128×8
Row decoder
256
Refresh controller
Refresh timer
Data output buffer (8)
Data input buffer (8)
I/O1~I/O8

■TC5564APL-15 051-1085-50 8192 Words×8 Bits CMOS Static RAM

Outward Form


38.0MAX
28
15
1
14
14.2MAX
2.54

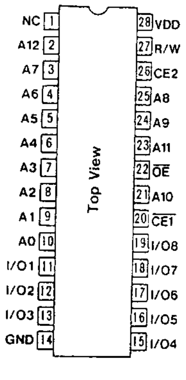
Outline

This IC is an asynchronous high speed CMOS static RAM of the 8192 words × 8 bits configuration, driven by a single 5V power supply.

Access Time

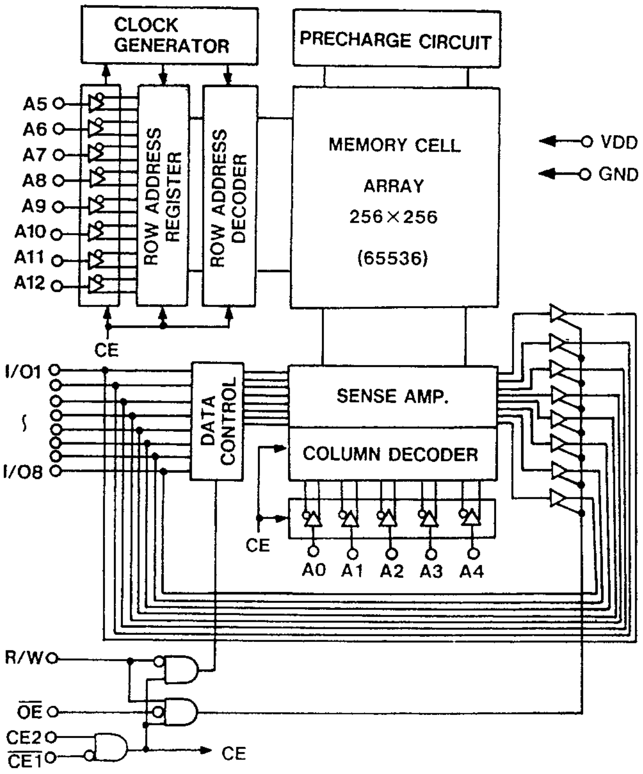
150ns

Terminal Connection


NC 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
I/O1 11
I/O2 12
I/O3 13
GND 14
Top View
28 VDD
27 R/W
26 CE2
25 A8
24 A9
23 A11
22 OE
21 A10
20 CE1
19 I/O8
18 I/O7
17 I/O6
16 I/O5
15 I/O4

A0~A12	Address Input
R/W	Read/Write Control Input
$\overline{\text{OE}}$	Output Enable Input
$\overline{\text{CE1}}$, CE2	Chip Enable Input
I/O1~I/O8	Data I/O
VDD	Power Terminal (+5V)
GND	Ground
N.C.	Not in use

Block Diagram

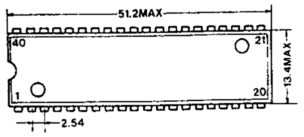

CLOCK GENERATOR
PRECHARGE CIRCUIT
A5
A6
A7
A8
A9
A10
A11
A12
ROW ADDRESS REGISTER
ROW ADDRESS DECODER
MEMORY CELL ARRAY 256×256 (65536)
VDD
GND
CE
I/O1
I/O8
DATA CONTROL
SENSE AMP.
COLUMN DECODER
CE
A0 A1 A2 A3 A4
R/W
OE
CE2
CE1
CE

Operation Mode

Operation mode	$\overline{\text{CE1}}$	CE2	$\overline{\text{OE}}$	R/W	I/O1~I/O8	POWER
READ	L	H	L	H	DOUT	IDDO
WRITE	L	H	*	L	DIN	IDDO
OUTPUT DISABLE	*	*	H	*	High-Z	IDDO
STANDBY	H *	* L	* *	* *	〃 〃	IDDS IDDS

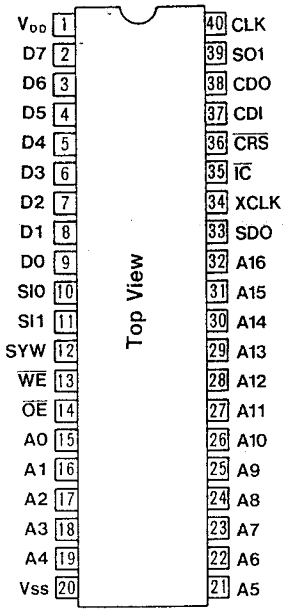
■YM3413 653-0198-75 Sound Field Creation DSP

Outward Form



51.2MAX
40
21
1
20
13.4MAX
2.54

Terminal Connection



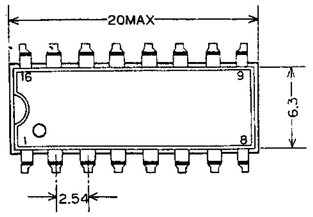
Top View
V_{DD} 1
D7 2
D6 3
D5 4
D4 5
D3 6
D2 7
D1 8
D0 9
SI0 10
SI1 11
SYW 12
$\overline{WE}$ 13
$\overline{OE}$ 14
A0 15
A1 16
A2 17
A3 18
A4 19
Vss 20
40 CLK
39 SO1
38 CDO
37 CDI
36 $\overline{CRS}$
35 $\overline{IC}$
34 XCLK
33 SDO
32 A16
31 A15
30 A14
29 A13
28 A12
27 A11
26 A10
25 A9
24 A8
23 A7
22 A6
21 A5

Terminal Description

Pin No.	Symbol	I/O	Function
1	V_{DD}	–	+5V voltage supply
2 ∫ 9	D7 ∫ D0	I/O	I/O pins connected to memory data bus (8 bit)
10	SI0	I	Serial data input
11	SI1		
12	SYW	I	System sync signal input
13	$\overline{\text{WE}}$	O	Read/write signal to memory input
14	$\overline{\text{OE}}$	O	Pin connected to memory OE terminal
15 ∫ 19	A0 ∫ A4	O	Outputs connected to memorys address bus
20	V_{ss}	–	GND 0V
21 ∫ 32	A5 ∫ A16	O	Outputs connected to memory address bus
33	SDO	O	Serial data output
34	XCLK	I	ACIA clock input
35	$\overline{\text{IC}}$	I	LDSP initial clear signal input
36	$\overline{\text{CRS}}$	I	CD data sync signal input
37	CDI	I	CD data input
38	CDO	O	CD data output
39	SO1	O	Serial data output
40	CLK	I	Master clock input

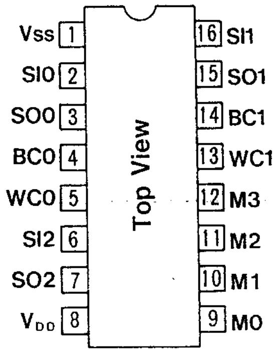
■YM3422 653-0198-77 Digital Signal Format Converter

Outward Form



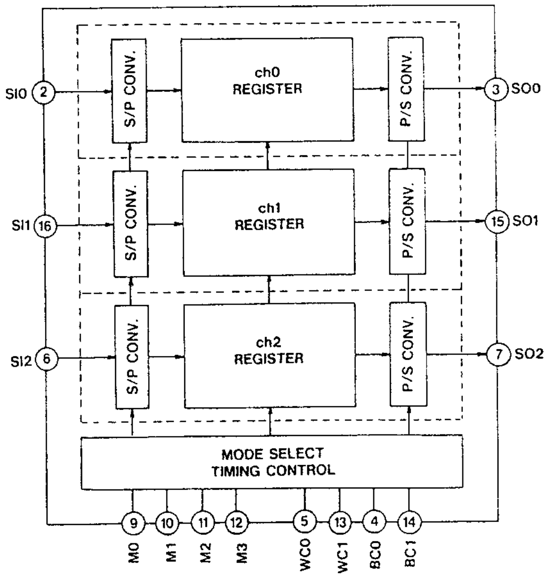
20MAX
16
9
1
8
6.3
2.54

Terminal Connection



Top View
Vss 1
SI0 2
SO0 3
BCO 4
WCO 5
SI2 6
SO2 7
V_{DD} 8
16 SI1
15 SO1
14 BC1
13 WC1
12 M3
11 M2
10 M1
9 M0

Block Diagram



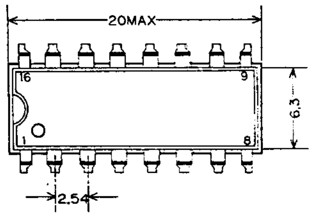
SI0 2
SI1 16
SI2 6
S/P CONV.
ch0 REGISTER
ch1 REGISTER
ch2 REGISTER
P/S CONV.
3 SO0
15 SO1
7 SO2
MODE SELECT
TIMING CONTROL
9 M0
10 M1
11 M2
12 M3
5 WCO
13 WC1
4 BCO
14 BC1

Terminal Description

Pin No.	Symbol	I/O	Function
1	Vss	–	GND terminal
2	SI0	I	Serial data input (ch 0)
3	SO0	O	Serial data output (ch 0)
4	BC0	I	Bit clock input
5	WC0	I	System synchronized signal input
6	SI2	I	Serial data input (ch 2)
7	SO2	O	Serial data output (ch 2)
8	V_{DD}	–	Voltage supply (+5V)
9 ∫ 12	M0 ∫ M3	I	Mode select signal
13	WC1	I	System synchronized signal input (Word clock)
14	BC1	I	Bit clock input
15	SO1	O	Serial data output (ch 1)
16	SI1	I	Serial data input (ch 1)

■YM3433 653-0198-78 2-Channel 8-Times Over-Sampling Digital Filter

Outward Form

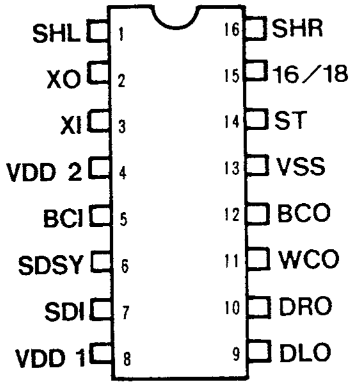


20MAX
16
9
1
8
6.3
2.54

Features

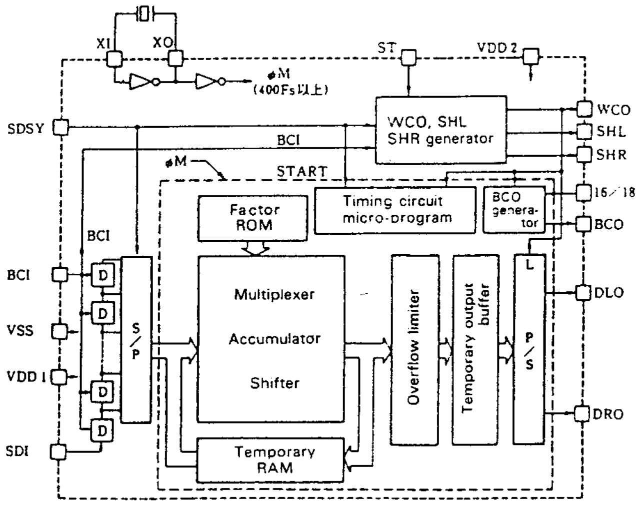
- ●This IC operates with a system clock independent from input serial signal so that it is compatible with any input signal with the input bit clock rate of 32Fs, 48Fs, 64Fs, 80Fs, 96Fs, 112Fs, 128Fs, 144Fs, 160Fs, 176Fs and 192Fs, without an additional circuit.
- ●Linear phase FIR filters are connected at three stages longitudinally.
  1st filter : 161st FIR filter
  2nd filter : 33rd FIR filter
  3rd filter : 17th FIR filter
- ●A built-in overflow limiter.
- ●Filter performance (8-times)
  Passband ripple ························0~0.4535×Fs : ±0.002dB or less
  Stopping passband attenuation······0.5465×Fs~7.4535×Fs : −70dB or more
- ●16-bit and 18-bit output is selectable.
- ●1DAC (4-time) and 2DAC (8-time) is selectable.
- ●CMOS process and signale 5V power supply.

Terminal Connection



SHL 1
XO 2
XI 3
VDD 2 4
BCI 5
SDSY 6
SDI 7
VDD 1 8
16 SHR
15 16/18
14 ST
13 VSS
12 BCO
11 WCO
10 DRO
9 DLO

Block Diagram



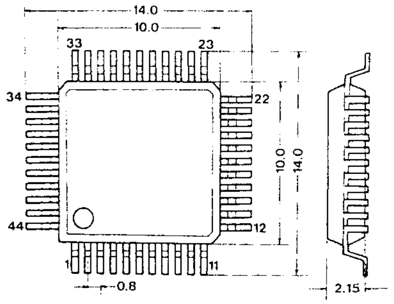
XI
XO
ST
VDD 2
φM
(400Fs以上)
SDSY
BCI
WCO, SHL
SHR generator
WCO
SHL
SHR
φM
START
Factor ROM
Timing circuit
micro-program
BCO
genera-
tor
16/18
BCO
BCI
D
S/P
Multiplexer
Accumulator
Shifter
Overflow limiter
Temporary output buffer
L
P/S
DLO
DRO
VSS
VDD 1
SDI
Temporary RAM

Terminal Description

Pin No.	Symbol	I/O	Function
1	SHL	O	1DAC (ST="L") : Lch degricher signal 2DAC (ST="H") : L/Rch degricher signal
2 3	XO XI	O I	XI−XO oscillates crystal of system clock. External clock can be directly input to XI.
4	VDD2	–	+5V power terminal for crystal oscillation and degricher signals.
5	BCI	I	A terminal receives bit and clock of input data.
6	SDSY	I	Clock input terminal which indicates L/Rch and input timing of input data.
7	SDI	I	Data input terminal.
8	VDD1	–	+5V power terminal.
9	DLO	O	1DAC (ST="L") : L/Rch data output terminal 2DAC (ST="H") : Lch data output terminal
10	DRO	O	Rch data output terminal
11	WCO	O	Word clock output terminal for output data DLO and DRO.
12	BCO	O	Bit clock output terminal for output data DLO and DRO.
13	VSS	–	GND terminal.
14	ST	I	1DAC/2DAC select terminal (1DAC="L", 2DAC="H")
15	16/18	I	Output data bit select terminal (16 bits="L", 18 bits="H")
16	SHR	O	1DAC (ST="L") : Rch degricher signal

■YM3436 653-0198-79 Digital Audio Interface Receiver

Outward Form



14.0
10.0
33
23
34
22
44
12
1
11
10.0
14.0
0.8
2.15

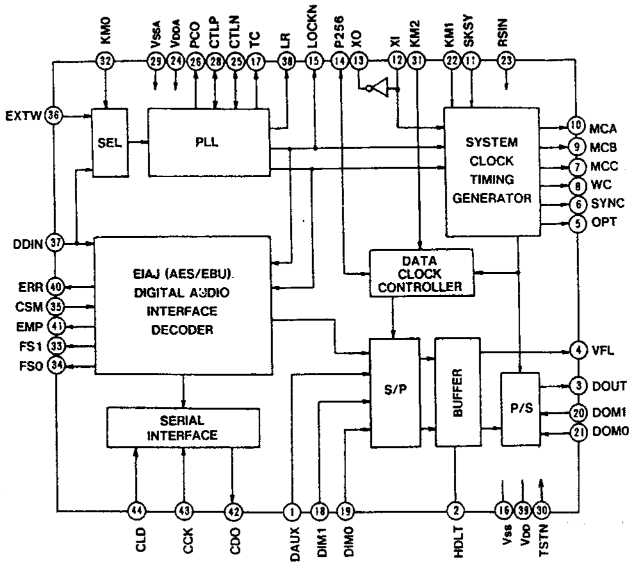
Outline

This IC is an LSI which receives and demodulates digital audio interface format signal compatible with EIAJ CP-340 and AES/EBU.

Features

- ●Compatible with input of digital audio signal interface signal but also A/D input and asynchronous input.
- ●Built-in VCO enables configuration of PLL circuit synchronizing with external input.
- ●Demodulates digital audio interface signal to output 24-bit 2-channel audio data and control data.
- ●Supplies clocks to downstream LSIs as the clock master.
- ●Built-in asynchronous buffer is compatible with twin PLL.
- ●Detects transmission and reception error, holds previous values and processes muting error etc.
- ●Decodes and outputs validity flag, channel status and user data as control data. Data can be also read by interfacing this with microprocessor.
- ●Single 5V power supply.

Block Diagram

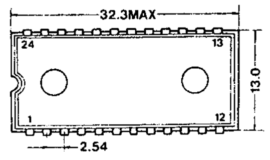

KMO
VSSA
VDDA
PCO
CTLP
CTLN
TC
LR
LOCKN
P256
XO
XI
KM2
KM1
SKSY
RSIN
EXTW
SEL
PLL
SYSTEM CLOCK TIMING GENERATOR
MCA
MCB
MCC
WC
SYNC
OPT
DDIN
ERR
CSM
EMP
FS1
FSO
EIAJ (AES/EBU) DIGITAL AUDIO INTERFACE DECODER
DATA CLOCK CONTROLLER
S/P
BUFFER
P/S
VFL
DOUT
DOM1
DOMO
SERIAL INTERFACE
CLD
CCK
CDO
DAUX
DIM1
DIMO
HDLT
Vss
VDD
TSTN

Terminal Description

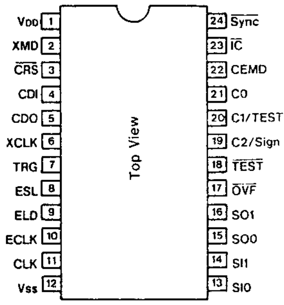
Pin No.	Symbol	I/O	Function
1	DAUX	I	Auxiliary input of audio data
2	HDLT	O	Output of asynchronous buffer operation flag
3	DOUT	O	Output of audio data
4	VFL	O	Output of validity flag
5	OPT	O	Output of DAC synchronous signal (fs)
6	SYNC	O	Output of DSP synchronous signal (fs)
7	MCC	O	Output of bit clock (64fs)
8	WC	O	Output of word clock (fs)
9	MCB	O	Output of bit clock (128fs)
10	MCA	O	Output of bit clock (256fs)
11	SKSY	I	Input of clock synchronous control
12	XI	I	Connection of crystal oscillator or input of external clock (256fs)
13	XO	O	Connection of crystal oscillator
14	P256	O	Output of VCO clock
15	LOCKN	O	Output of PLL lock flag ("L" : Locked, "H" : Unlocked)
16	VSS	–	Ground (logic)
17	TC	O	LSI test terminal (normally not connected)
18	DIM1	I	Selection of data input mode 1
19	DIMO	I	Selection of data input mode 0
20	DOM1	I	Selection of data output mode 1
21	DOMO	I	Selection of data output mode 0
22	KM1	I	Selection of clock mode 1 ("H" : Automatic select of PLL, "L" : Fixed to XI)
23	RSIN	I	Input of system reset (active Low)
24	VDDA	–	+5V power supply (with VCO externally connected to VDD)
25	CTLN	I	Input of VCO control
26	PCO	O	Comparison and output of PLL phase
27	(NC)	–	(Not connected externally)
28	CTLP	I	Input of VCO adjustment
29	VSSA	–	Ground (with VCO connected to VSS externally)
30	TSTN	I	LSI test terminal (normally not connected)
31	KM2	I	Selection of clock mode 2 ("H" : Synchronous with XI, "L" : Synchronous with PLL)
32	KMO	I	Selection of clock mode 0 ("H" : Input of EXTW, "L" : Input of DDIN)
33	FS1	O	Indication and output of channel status sampling frequency 1
34	FSO	O	Indication and output of channel status sampling frequency 0
35	CSM	I	Selection of channel status user data output mode
36	EXTW	I	Auxiliary input of externally synchronous word clock
37	DDIN	I	Input of EIAJ (AES/EBU) digital audio interface signal
38	LR	O	Output of PLL word clock
39	VDD	–	+5V power supply (logic)
40	ERR	O	Output of data error flag
41	EMP	O	Output of channel status emphasis control code
42	CDO	O	Output of microprocessor interface data
43	CCK	I	Output of microprocessor interface clock
44	CLD	I	Input of microprocessor interface load

■YM6104 653-0198-76 Digital Equalizer

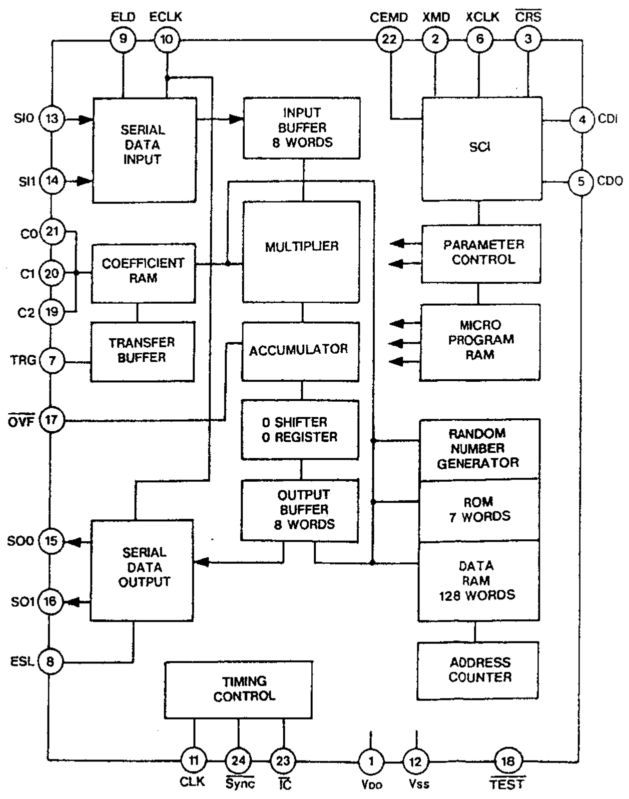
Outward Form


32.3MAX
24
13
1
12
13.0
2.54

Terminal Connection


Vdd 1
XMD 2
CRS 3
CDI 4
CDO 5
XCLK 6
TRG 7
ESL 8
ELD 9
ECLK 10
CLK 11
Vss 12
24 Sync
23 IC
22 CEMD
21 CO
20 C1/TESTM
19 C2/Sign
18 TEST
17 OVF
16 SO1
15 SOO
14 SI1
13 SIO
Top View

Block Diagram

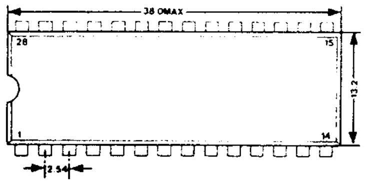

ELD
ECLK
CEMD
XMD
XCLK
CRS
SIO
SI1
CO
C1
C2
TRG
OVF
SOO
SO1
ESL
SERIAL DATA INPUT
INPUT BUFFER 8 WORDS
SCI
CDI
CDO
COEFFICIENT RAM
MULTIPLIER
PARAMETER CONTROL
TRANSFER BUFFER
ACCUMULATOR
MICRO PROGRAM RAM
0 SHIFTER 0 REGISTER
RANDOM NUMBER GENERATOR
OUTPUT BUFFER 8 WORDS
ROM 7 WORDS
SERIAL DATA OUTPUT
DATA RAM 128 WORDS
TIMING CONTROL
ADDRESS COUNTER
CLK
Sync
IC
Vdd
Vss
TEST

Terminal Description

Pin No.	Symbol	I/O	Function
1	V_{DD}	I	+5V power supply
2	XMD	I	Switches CDI input to either synchronous mode (1 : 1) "L" or asynchronous mode (Start-stop synchronous system 16 : 1) "H"
3	$\overline{\text{CRS}}$	I	Initializes SCI interface
4	CDI	I	SCI input for setting micro program, factor and control register
5	CDO	O	SCI output for setting micro program, factor and control register
6	XCLK	I/O	Input-output clock for CDI and CDO
7	TRG	I	Determines parameter transfer timing from transfer buffer to factor RAM when external trigger is selected
8	ESL	I	Enters output timing into SOO and SO1 when EXT clock is selected
9	ELD	I	Enters input timing into SIO and SI1 when EXT clock is selected
10	ECLK	I/O	Enters input-output clock for SIO, SOO and SO1 when EXT clock is selected
11	CLK	I	Master clock input
12	Vss	I	Ground
13, 14	SIO, SI1	I	16 bits serial input
15, 16	SOO, SO1	O	16 bits serial output
17	$\overline{\text{OVF}}$	O	Over flow detect
18	$\overline{\text{TEST}}$	I	Used for testing Usually connected to +5V
19	C2/Sign	O	Outputs bit 2 of factor RAM while delaying it by 1 bit. Used as a timing signal Monitors sign bit of accumulator by setting test register (When factor RAM is used as a timing signal, effective bit number of factor decreases)
20	C1/TESTM	O	Outputs bit 1 of factor RAM while delaying it by 1 bit. Used as a timing signal Switches to test output of multiplier by setting test register
21	CO	O	Outputs bit 2 of factor RAM while delaying it by 1 bit. Can be used as a timing signal
22	CEMD	I	Turns OFF CE of SCI input CE ON : "H" CE OFF : "L"
23	$\overline{\text{IC}}$	I	Initializes DEQ operation
24	$\overline{\text{Sync}}$	I	Synchronous signal of system

■µPD27C512C-15 653-0198-13 65536 Words×8 Bits CMOS One Time PROM

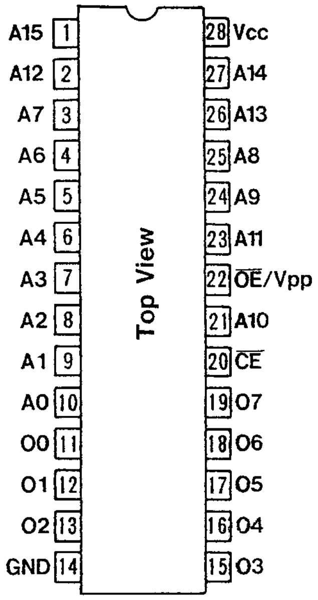
Outward Form


38.0MAX
28
15
1
14
13.2
2.54

Outline

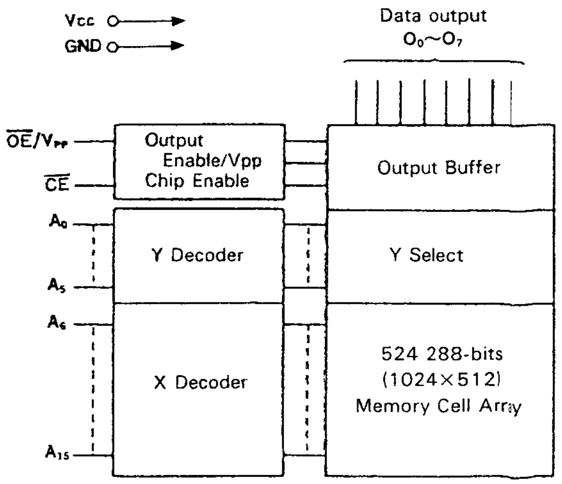
This IC is an electrically programmable one-time ROM of 65536 works×8 bits (524288 bits).

Terminal Connection


A15 1
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
A2 8
A1 9
A0 10
O0 11
O1 12
O2 13
GND 14
28 Vcc
27 A14
26 A13
25 A8
24 A9
23 A11
22 OE/Vpp
21 A10
20 CE
19 O7
18 O6
17 O5
16 O4
15 O3
Top View

A0～A15	Address input
O0～O7	Data output
$\overline{\text{CE}}$	Input of chip enable
$\overline{\text{OE}}$/Vpp	Input of output enable / Vpp
Vcc	Power supply
GND	Ground

Block Diagram


Vcc
GND
Data output
O0～O7
OE/Vpp
CE
Output Enable/Vpp Chip Enable
Output Buffer
A0
A5
A6
A15
Y Decoder
Y Select
X Decoder
524 288-bits (1024×512) Memory Cell Array

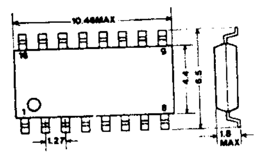
Operation Mode

Mode \ Terminal	$\overline{\text{CE}}$	$\overline{\text{OE}}$/Vpp	Vcc	O_0～O_7
READ	V_{IL}	V_{IL}	+5V	Data output
OUTPUT DISABLE	V_{IL}	V_{IH}	+5V	High impedance
STANDBY	V_{IH}	X	+5V	High impedance
PROGRAM	V_{IL}	+12.5V	+6V	Data input
PROGRAM VERIFY	V_{IL}	V_{IL}	+6V	Data output
PROGRAM INHIBIT	V_{IH}	+12.5V	+6V	High impedance

X : V_{IL} or V_{IH}

■µPD4053BG 658-0188-83 Triple 2-Channel Multiplexer/Demultiplexer

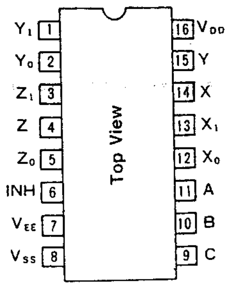
Outward Form



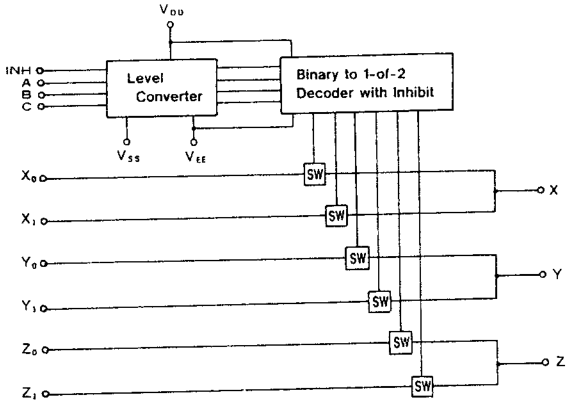
Outline

This IC is a multiplexer of three 2-channel configuration consisting of the level converter, decoder and analog switch. When digital signal is received by the control terminal, a switch associated with the channel is turned ON.

Terminal Connection



Block Diagram



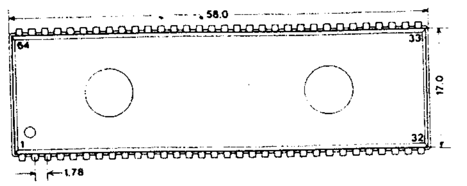
Truth Table

Control Input				"ON" Channel
INHIBIT	C	B	A	
L	L	L	L	Z_0, Y_0, X_0
L	L	L	H	Z_0, Y_0, X_1
L	L	H	L	Z_0, Y_1, X_0
L	L	H	H	Z_0, Y_1, X_1
L	H	L	L	Z_1, Y_0, X_0
L	H	L	H	Z_1, Y_0, X_1
L	H	H	L	Z_1, Y_1, X_0
L	H	H	H	Z_1, Y_1, X_1
H	X	X	X	NONE

H : High level
L : Low level
X : H or L

■HD63B01Y 653-0198-08 DSP Controller

Outward Form



Terminal Description

Pin No.	Symbol	I/O	Function
1	Vss	–	Ground
2	XTAL	–	Oscillation circuit
3	EXTAL	–	Oscillation circuit
4	MP0	–	Mode program input Fixed to "H"
5	MP1	–	Mode program input Fixed to "L"
6	$\overline{RES}$	–	Reset input (Negative logic)
7	$\overline{STBY}$	–	Stand-by input (Negative logic)
8	$\overline{NMI}$	–	$\overline{NMI}$ input (Negative logic) Used for resetting equipment
9	CEC	O	LCD driver (C) chip enable
10	CDI	I	Bit 0 input of DEQ coefficient RAM
11	LCLK	O	Clock for LCD driver
12	DG	I	Communication input
13	DATA	O	Communication output
14	CEA	O	DA control output
15	CEB	O	DA control output
16 ∫ 18	DI0 ∫ DI2	O	Key signal output
19	DI3	I	Overflow input pull-down
20	DI4	I	Halt input
21 ∫ 24	K0 ∫ K3	I	Key signal input
25	CONTROL	I	DA control input
26	EMP	I	Digital in emphasis input
27	ERR	I	Digital in error input
28	FS0	I	Sampling frequency select input
29	FS1	I	
30	DI	O	Data for volume IC
31	VCLK	O	Clock for volume IC
32	CE	O	Chip enable for volume IC
33	Vcc	–	Power source
34 ∫ 41	A15 ∫ A8	–	Address bus
42	Vss	–	Ground
43 ∫ 50	A7 ∫ A0	–	Address bus
51 ∫ 58	D7 ∫ D0	–	Data bus
59 ∫ 61	NC	–	Not in use
62	$\overline{WR}$	O	Write signal output
63	$\overline{RD}$	O	Read signal output
64	E	O	System clock output

■PARTS LIST:

◎Electrical section

●Main P. W. B section

NOTE: •‾•=•TO FROM•

REF NO.	PART NO.	DISCRIPTION	Q' TY
BZ301	653-0198-16	Buzzer	1
C301. 304. 305. 308. 309. 312. 374. 375	179-3363-32	Electorolytic capacitor 16V-33µF	8
C302. 303	653-0197-67	Chip ceramic capacitor 50V-220PF	2
C306. 307. 310. 311	177-4722-05	Chip ceramic capacitor 50V-4700PF K	4
C316. 317. 376‾379	183-3363-42	Electorolytic capacitor 16V-33µF	6
C330. 331. 342. 343	183-2253-62	Electorolytic capacitor 50V-2. 2µF	4
C333. 334. 337. 338	183-1063-32	Electorolytic capacitor 16V-10µF	4
C361. 364. 381. 385. 394. 396‾401. 418‾420	653-0197-51	Chip ceramic capacitor 25V-0. 1µF	14
C365	653-0197-69	Chip ceramic capacitor 50V-1000PF	1
C366. 688	179-1063-32	Electorolytic capacitor 16V-10µF	2
C373	653-0197-77	Electorolytic capacitor 5. 5V-2200µF	1
C393	653-0197-72	Electorolytic capacitor 25V-33µF	1
C410. 682. 690	653-0197-70	Chip ceramic capacitor 50V-0. 01µF	3
C415. 626. 681	653-0197-65	Chip ceramic capacitor 25V-1µF	3
C416. 417	653-0197-62	Chip ceramic capacitor 50V-22PF CH J	2
C421‾424	653-0197-68	Chip ceramic capacitor 50V-560PF	3
C628	653-0197-63	Chip ceramic capacitor 50V-1000PF CH J	1
C629. 656. 657	177-1042-05	Chip ceramic capacitor 50V-0. 1UF K	3
C640	653-0197-61	Polyster capacitor 50V-0. 027µF J	1
C641	653-0197-76	Electorolytic capacitor 25V-2200µF	1
C647. 650	653-0197-74	Electorolytic capacitor 25V-470µF	2
C648. 651. 652. 654. 680. 683. 685. 686	653-0197-64	Chip ceramic capacitor 25V-0. 47µF	8
C649. 655	043-0408-00	Electorolytic capacitor 16V-330µF	2
C653	653-0197-75	Electorolytic capacitor 10V-1800µF	1
C660. 673	042-0280-00	Electorolytic capacitor 16V-1000µF	2
C663	653-0197-73	Electorolytic capacitor 50V-1000µF	1
C672. 691	653-0197-71	Electorolytic capacitor 16V-47µF	2
C684	653-0197-66	Chip ceramic capacitor 50V-1000PF B	1
CB301	653-0198-19	PH base pin 2P	1
CB302. 303	653-0198-20	VH base pin 7P	2
CB601	653-0198-18	VH base pin 4P	1
D312	653-0198-32	Chip diode HZK5LL-B or HZK5LL-B	1
D346‾351. 654	658-0188-91	Diode MA221	7
D352‾355. 356. 357. 649	653-0198-28	Diode array HMS123	7
D356‾359 (NO. 1‾2500)	001-0294-00	Diode 1SS133	4
D601. 604	653-0198-27	Photo capler	2
D602	653-0198-31	Chip diode RLZJ10C	1
D603. 607. 609	653-0198-26	Diode HRP32	3
D605	653-0198-30	Chip diode RLZ5. 6B	1
D608	653-0198-29	Chip diode RLZ5. 6A	1
D610	653-0198-25	Diode 31DQ04	1
D650. 651	653-0198-24	Diode 1SR35-100AT-93X	2
D653	001-0188-00	Diode 1S1885	1
IC301	653-0197-90	IC µPC4570G2-T1	1
IC302. 303	653-0197-91	IC µPC812G2	2
IC305. 307	653-0069-77	IC M5238FP	2
IC308. 309	653-0198-15	IC LC7535	2
IC312	653-0198-08	IC HD63B01Y or HD63B03YP	1
IC312	653-0198-11	IC HD63B01Y0RL73P	1
IC313	653-0198-12	IC µPD27C512D-15 or µPD27C512EC . µPD27C 512C	1
IC315	653-0197-94	IC M62021L	1
IC316	051-1085-50	IC TC5564APL-15	1
IC317	653-0198-06	IC µPD74HC166G-T1	1
IC318	653-0197-98	IC µPD74HC273G-T1	1
IC322. 323	653-0197-99	IC µPD74HC00G or MN74HC00S . LC74HC00M	2
IC324	653-0198-03	IC µPD74HC04G or MN74HC04S . LC74HC04M	1
IC325. 327	653-0198-07	IC µPD74HC02G-T1	2

REF NO.	PART NO.	DISCRIPTION	Q' TY
IC326	051-1321-00	IC NJM79L05A or AN79L05	1
IC604	653-0197-95	IC MB3776	1
IC609	653-0197-96	IC μPC24M12F	1
IC610	653-0197-97	IC μPC79M12F	1
IC611	653-0197-92	IC μPC1093J	1
J301¯304. 308	117-0000-00	Chip jumper	5
L601	653-0197-81	Choke coil 90μH	1
L602	653-0197-80	Coil 470μH	1
L603	653-0197-79	Coil 18μH	1
L604. 605	653-0197-78	Coil 4.7μH	2
PJ301	653-0198-17	Pin jack 2P	1
Q301. 601	125-2020-02	Transistor DTC114EK	2
Q303¯306	102-3326-02	Transistor 2SC3326B	4
Q314	125-2007-03	Transistor DTC114ES	1
Q315. 316	102-1815-25	Transistor 2SC1815Y	2
Q317. 603. 612. 615	653-0069-54	Transistor 2SC2412 (Q. R. S)	4
Q601	658-0188-64	Transistor 2SB560 (F. E)	1
Q607	103-1266-17	Transistor 2SD1266 (P. Q)	1
Q608	653-0198-22	F. E. T 2sk1095	1
Q614	125-0014-02	Transistor DTA114EK	1
Q615 (NO. 1¯2500)	653-0198-23	Transistor 2SC2603	1
R301. 306	653-0197-85	Chip resistor (METAL) 470Ω	2
R302. 305. 409¯412	117-4741-10	Chip resistor 470KΩ	6
R303. 304	653-0197-86	Chip resistor (METAL) 22KΩ	2
R308. 311. 314. 317. 626. 654. 668	117-2221-10	Chip resistor 2.2KΩ	7
R309. 310. 315. 316. 383. 385. 603. 604	117-1031-10	Chip resistor 10KΩ	8
R322. 371. 374. 398. 403. 417. 418. 665	117-4721-10	Chip resistor 4.7KΩ	8
R357	653-0197-87	Resistor array 4.7KΩ×4	1
R375. 378. 379	653-0197-89	Resistor array 4.7KΩ×8	3
R376. 432. 436	117-1051-10	Chip resistor 1MΩ	3
R377	117-1141-10	Chip resistor 110KΩ	1
R380. 602. 605	117-1021-10	Chip resistor 1KΩ	3
R381	117-1531-10	Chip resistor 15KKΩ	1
R382. 384	117-1321-10	Chip resistor 1.3KΩ	2
R408	116-2201-10	Chip resistor 22Ω	1
R413	653-0197-84	Chip resistor 4.7Ω	1
R419¯426	116-1011-10	Chip resistor 100Ω	8
R427¯430	117-1011-10	Chip resistor 100Ω	4
R431	653-0197-88	Resistor array 100KΩ×4	1
R433¯435	116-1051-10	Chip resistor 1MΩ	3
R601	117-2201-10	Chip resistor 22Ω	1
R606. 607. 609. 610. 611. 666	117-4731-10	Chip resistor 47KΩ	6
R608	117-4701-10	Chip resistor 47Ω	1
R624	116-2211-10	Chip resistor 220Ω	1
R625	653-0197-83	Chip resistor 4.7Ω	1
R627	117-1521-10	Chip resistor 1.5KΩ	1
R628	117-3311-10	Chip resistor 330Ω	1
R642	117-5121-10	Chip resistor 5.1KΩ	1
R651	114-6811-11	Film resistor (OM) 1W-680Ω	1
R653	116-1001-10	Chip resistor 10Ω	1
R667	117-2721-10	Chip resistor 2.7KΩ	1
R673	117-1041-10	Chip resistor 100KΩ	1
R691	116-1511-10	Chip resistor 150Ω	1
T601	653-0197-82	Trans	1
VR601	658-0188-53	Semi valiable resistor 1KΩ B	1
XL301	653-0198-21	Crystal	1

●DSP P.W.B section

REF NO.	PART NO.	DISCRIPTION	Q' TY
C130. 133. 198. 201	653-0198-58	Chip ceramic capacitor 50V-220PF CH	8
C16. 18	653-0198-48	Polyster capacitor 50V-3300PF J	2
C17. 20	653-0198-53	Chip ceramic capacitor 50V-100PF	2
C177. 178. 187	183-3363-42	Electorolytic capacitor 16V-33μF	3
C1¯6. 8¯14. 103. 104. 107. 108. 119. 120. 151. 172. 184. 185. 188¯191	653-0198-54	Chip ceramic capacitor 50V-120PF	27
C204	653-0198-52	Ceramic capacitor 25V-1.5μF	1
C21. 22. 192¯195. 197	653-0197-70	Chip ceramic capacitor 50V-0.01μF	7
23. 29. 33. 34. 36¯38. 40. 42¯44. 46. 54. C57. 76. 134. 135. 141. 142. 167. 169. 170. 179. 180. 182. 186. 196. 202. 203	653-0197-51	Chip ceramic capacitor 25V-0.01μF	29
C24. 26. 92¯95. 121¯124. 183	179-3363-32	Electorolytic capacitor 16V-33μF	11
C25. 30. 136¯138. 143¯147	653-0198-55	Chip ceramic capacitor 16V-0.47μF	10
C27. 165. 175	653-0197-65	Chip ceramic capacitor 25V-1μF	3
C28. 31	179-1063-32	Electorolytic capacitor 16V-10μF	2
C51. 52	653-0198-56	Chip ceramic capacitor 50V-22PF CH	2
C53	653-0198-50	Polyster capacitor 50V-0.022μF J	1
C55. 56	653-0198-57	Chip ceramic capacitor 50V-27PF CH	2
C58	183-1063-32	Electorolytic capacitor 16V-10μF	1
C78¯81	653-0198-51	Polyster capacitor 50V-0.068μF J	4
C82¯85	653-0198-49	Polyster capacitor 50V-5600PF J	4
C87¯90	653-0198-47	Polyster capacitor 50V-2400PF J	4
CB1. 2	653-0198-82	PH base pin 3P	2
CB3	653-0198-86	PH base pin 8P	1
CB4. 6	653-0198-83	PH base pin 5P	2
CB5	653-0198-84	PH base pin 6P	1
CB7	653-0198-85	PH base pin 7P	1
D1	653-0198-28	Diode array HMS123	1
IC1. 28. 29	653-0197-90	IC μPC4570G2-T1	3
IC10. 13	653-0198-72	IC TC51832FL-10	2
IC11	653-0198-77	IC YM3422	1
IC14. 15	653-0198-78	IC YM3433	2
IC17	653-0198-66	IC μPD74HC74G or MN74HC74S . LC74HC74M	1
IC19	653-0198-70	IC μPD74HC164G-T1	1
IC23. 27	653-0198-69	IC μPD74HCU04G-T1	2
IC24	653-0198-79	IC YM3436 (AF)	1
IC25	653-0197-99	IC μPD74HC00G or MN74HC00M . LM74HC00M	1
IC26	653-0198-07	IC μPD74HC02G-T1	1
IC3	051-1290-00	IC AN78N05	1
IC31. 32	653-0069-77	IC M5238FP	2
IC33. 37. 42	658-0188-83	IC UPD4053BG	3
IC34. 38	653-0198-73	IC PCM61P	2
IC39	653-0198-71	IC μPD74HC123G-T1	1
IC4	051-1321-00	IC NJM79L05A or AN79L05	1
IC41	653-0198-65	IC AN79N06	1
IC5	653-0198-74	IC AK5339-VP	1
IC6. 7	653-0198-76	IC YM6104	2
IC9. 12	653-0198-75	IC YM3413	2
J1¯10	117-0000-00	Chip jumper	11
JK1	653-0198-81	Optical receiving module	1
L1	653-0198-59	Coil 220μH	1
Q1	658-0188-06 658-0188-62 653-0198-89	Transistor 2SA933S (Q. R) Transistor 2SA1115 (E. F) Transistor 2SA1309A (Q. R. S)	1
Q2¯5	102-2878-00 102-3327-00	Transistor 2SC2878 (A. B) Transistor 2SC3327 Transistor 2SD1915 (F)	4
R1. 5. 7. 8. 13. 15	653-0069-09	Film resistor 1Ω	6
R10. 11. 36. 37. 39. 40. 48. 49. 51. 52	117-1021-10	Chip resistor 1KΩ	10

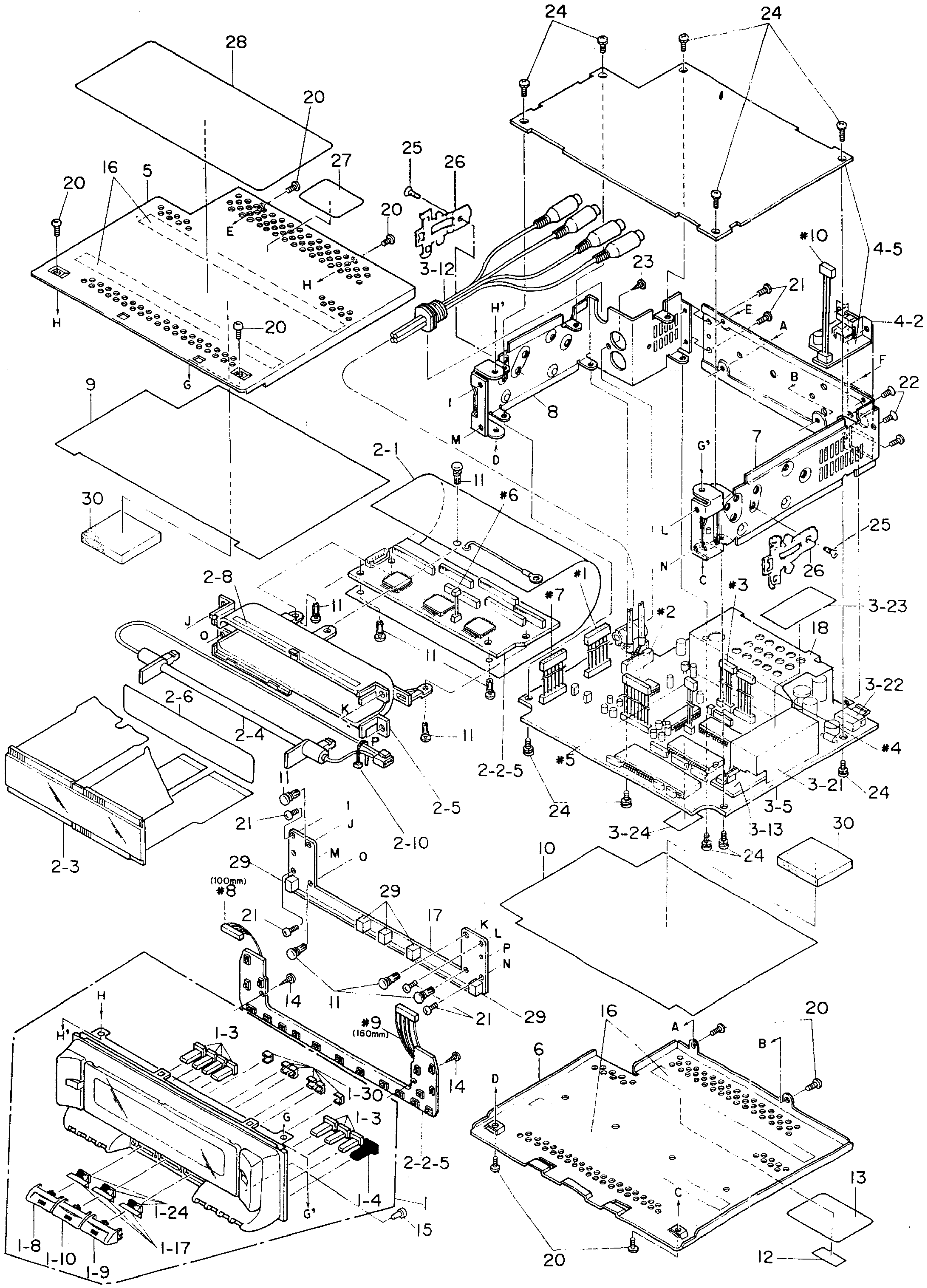
REF NO.	PART NO.	DISCRIPTION	Q' TY
R104	117-2201-10	Chip resistor 22Ω	1
R14. 16	117-5101-10	Chip resistor 51Ω	2
R17	117-1001-10	Chip resistor 10Ω	1
R2. 6	653-0198-62	Chip resistor (METAL) 3. 9KΩ	2
R21. 32	117-2211-10	Chip resistor 220Ω	2
R22. 31	117-1051-10	Chip resistor 1MΩ	2
R23. 87. 105~108	117-8211-10	Chip resistor 820Ω	6
R29	117-2401-10	Chip resistor 24Ω	1
R3. 4	653-0198-63	Chip resistor (METAL) 10KΩ	2
R33. 34	117-4721-10	Chip resistor 4. 7KΩ	2
R35. 38. 47. 50	117-4711-10	Chip resistor 470Ω	4
R41. 45. 54. 57	117-4741-10	Chip resistor 470KΩ	4
R42. 44. 53. 56	117-1811-10	Chip resistor 180Ω	4
R43. 46. 55. 58	117-1031-10	Chip resistor 10KΩ	4
R75. 88	117-1041-10	Chip resistor 100KΩ	2
R76~79	653-0198-60	Chip resistor 1. 5KΩ	4
R80~83	653-0198-61	Chip resistor 1. 8KΩ	4
R89	117-5631-10	Chip resistor 56KΩ	1
R9. 12	653-0198-64	Chip resistor (METAL) 15KΩ	2
R93. 94	117-5641-10	Chip resistor 560KΩ	2
R95~100. 103	653-0197-84	Chip resistor 4. 7Ω	7
SW1	653-0198-80	Slide switch	1
XL1	653-0198-88	Crystal 20MHz	1
XL2	653-0198-87	Crystal 11. 2896MHz	1

● Operation P.W.B section

REF NO.	PART NO.	DISCRIPTION	Q' TY
C769~771	653-0197-50	Chip ceramic capacitor 50V-680PF	3
C772~774	653-0197-51	Chip ceramic capacitor 25V-0. 1μF	3
CB701. 703. 706	653-0197-54	FPC connector 30P	3
CB702. 704. 705	653-0197-53	FPC connector 22P	3
CB707	653-0197-55	PH base pin 6P	1
D713~728	653-0197-57	Chip LED PG-1102W (GRN)	1
D729~744	653-0197-56	Chip LED AY-1102W (YEL)	1
IC718~720	051-0836-00	IC LC7582	3
R786~788	117-4731-10	Chip resistor 47KΩ	3
R790~797	116-2211-10	Chip resistor 220Ω	8
SW701~718	653-0197-52	Tact switch	18

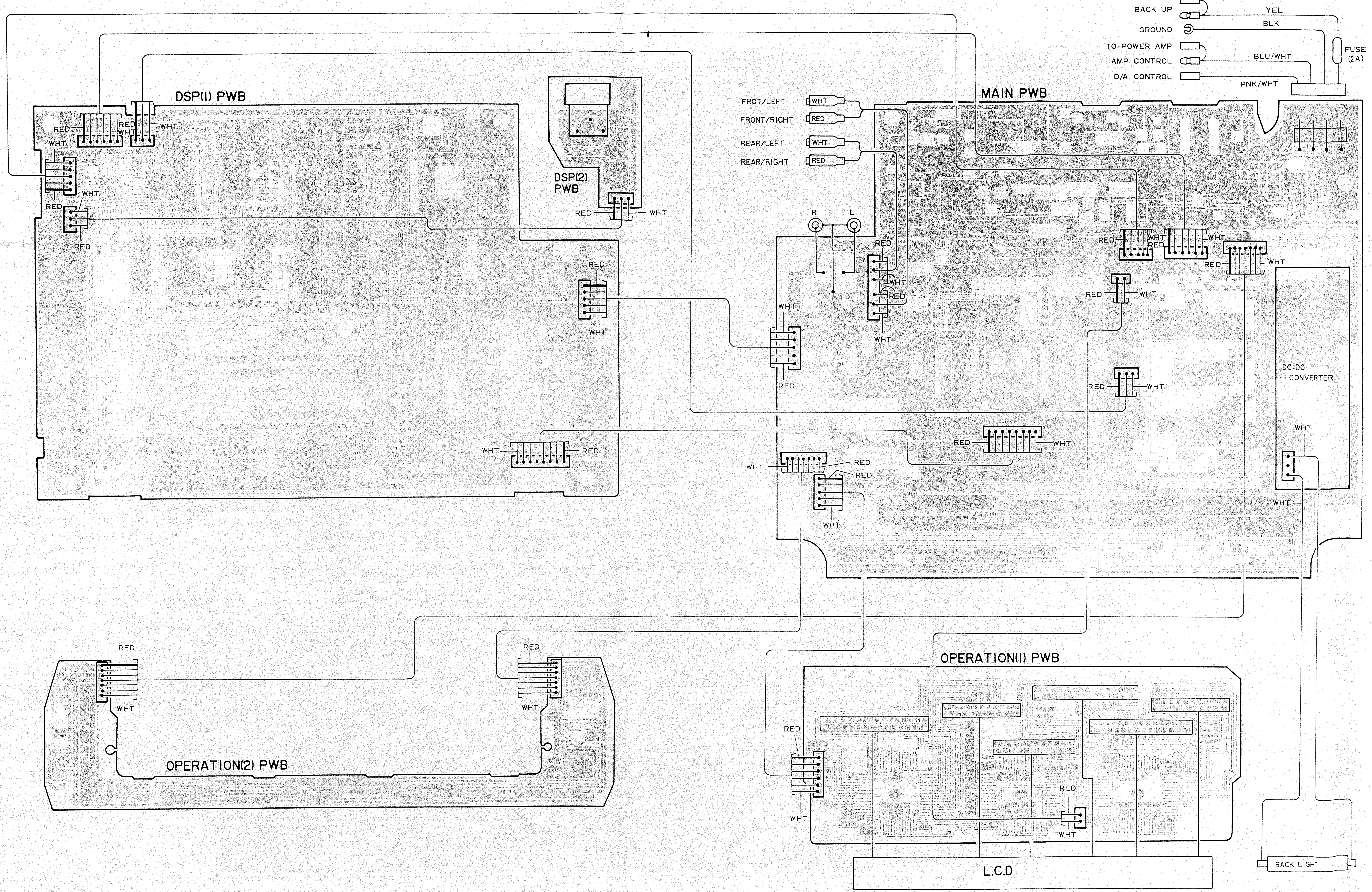
■EXPLODED VIEW • PARTS LIST:

◎Main section


28
24
24
20
27
16
5
20
25
26
20
E
H
H
3-12
23
21
H'
E
4-5
#10
4-2
A
F
20
B
9
G
22
I
8
M
D
7
G'
2-1
11
#6
30
11
25
L
#1
N
26
2-8
#7
#3
3-23
J
O
11
#2
18
11
K
3-22
2-6
2-4
P
11
2-2-5
#4
#5
24
3-21
24
11
2-3
21
I
J
2-10
2-5
24
3-5
3-24
3-13
30
M
O
29
(100mm)
#8
21
29
17
10
24
K
L
P
N
11
21
14
29
#9
(160mm)
16
20
A
B
H
H'
1-3
6
1-30
D
1-3
G
14
2-2-5
13
1-4
G'
1-24
1
15
C
1-8
1-10
1-9
1-17
20
12

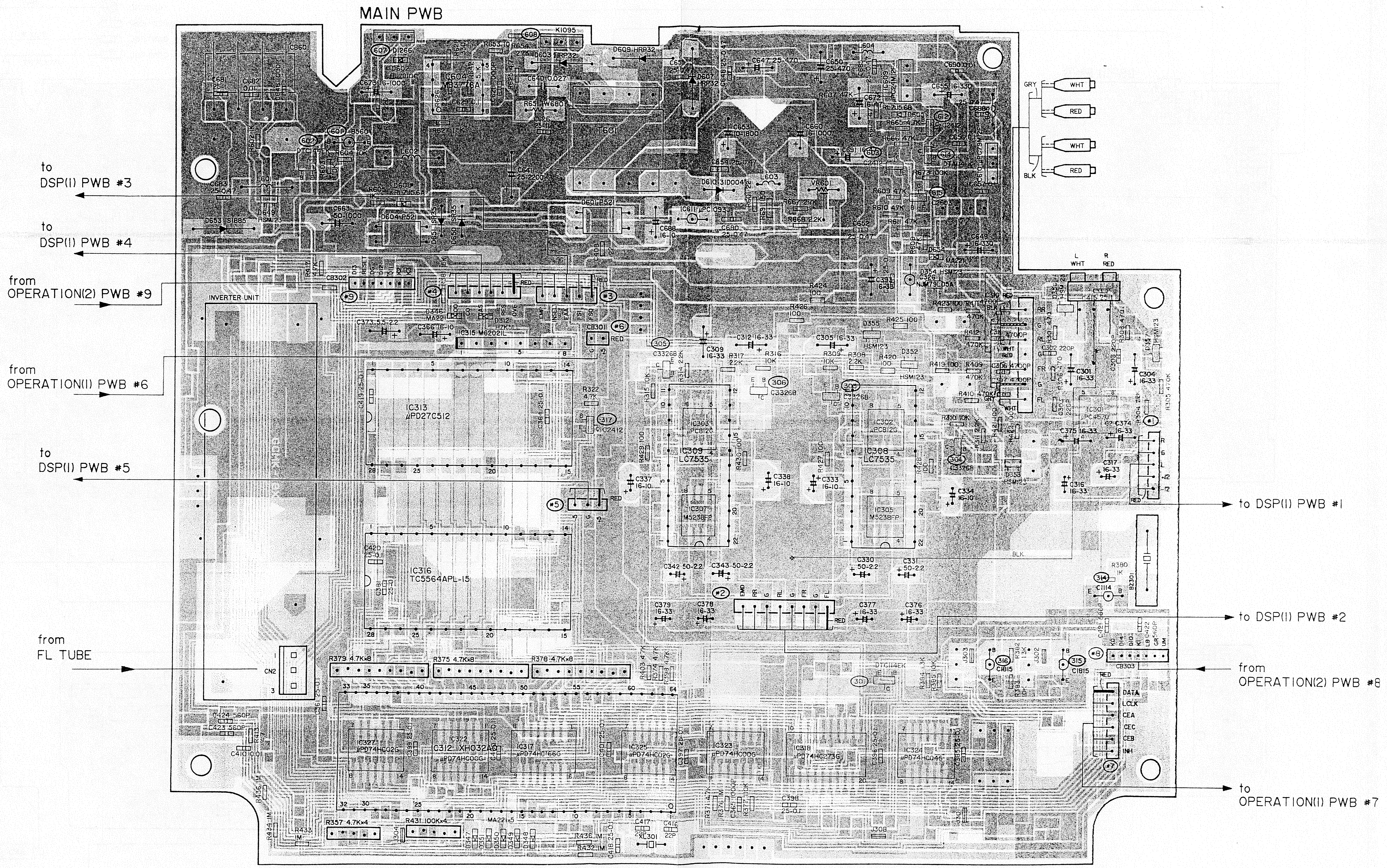
REF NO.	PART NO.	DISCRIPTION	Q' TY
1	653-0199-02	Escutchion ass'y	1
1-3	653-0197-26	Button	7
1-4	653-0197-27	Button (MEMO)	1
1-8	653-0197-29	Button (DSP-2)	1
1-9	653-0197-30	Button (EQ)	1
1-10	653-0197-31	Button (DSP-1)	1
1-17	653-0197-34	Rens	3
1-24	653-0197-35	Acetate cloth tape 10W	-
1-30	653-0197-37	Button cap	6
2-1	653-0197-44	Shielded plate ass'y	1
2-2-5	653-0197-59	P. W. B	1/2
2-3	653-0197-45	L. C. D	1
2-4	653-0197-46	Cold cathode lamp	1
2-5	653-0197-47	Reflector	1
2-6	653-0197-48	Sheet	1
2-8	653-0197-38	Double face tape	1
2-10	653-0197-49	Clamp	1
3-5	653-0198-36	Main P. W. B	1
3-12	854-2237-00	Output cord ass'y	1
3-13	653-0198-41	Inverter unit	1
3-21	653-0198-43	Shielded case I	1
3-22	653-0198-44	Sturnctur D	1
3-23	653-0198-45	Caution label	1
3-24	653-0198-46	Sheet	1
4-5	653-0198-91	DSP P. W. B	1
4-21	653-0198-93	Sturnctur	1
5	653-0197-05	Top cover	1
6	653-0197-06	Bottom cover	1
7	653-0197-07	Flame R	1
8	653-0197-08	Flame L	1
9	653-0197-09	Sheet BT	1
10	653-0197-10	Sheet BB	1
11	658-0187-94	Rivet #6888	5
12	653-0197-11 653-0199-08	Serial NO. label (small) Serial NO. label (leage)	1
13	653-0199-03 286-7672-00	Name plate (EE-982A-01) Name plate (EE-982B-01)	1
15	653-0197-28	Button (RESET)	1
16	653-0197-13	Double face tape	1
17	653-0197-14	Flame F	1
18	653-0197-15	Shielded case D	1
20	653-0197-16	Screw 3*6FNM33G	1
21	714-3006-85	Bind screw 3*6	1
22	653-0197-17	FT screw 2.6*FNM33G	1
23	653-0197-18	Bind P-tight 3*8	1
24	653-0197-19	Bind screw 3*6	11
25	653-0199-07	FT screw 5*8ZMCZ-N	1
26	750-2796-01	Spring	1
27	653-0199-04	Label (screw)	1
28	653-0199-05 653-0200-01	Label (EE-982A-01) Label (EE-982B-01)	1
29	653-0197-22	Damper 7/7/8	1
30	653-0197-23	Damper 50/50/5	1
31	653-0197-13	Double face tape	1
#1. #3	653-0198-37	PH connector ass'y 5P	1
#2	653-0198-40	PH connector ass'y 8P	1
#4	653-0198-39	PH connector ass'y 6P	1
#5	653-0198-34	Main connector ass'y	1
#6	653-0197-60	PH connector ass'y	1
#7	653-0198-38	PH connector ass'y 6P	1
#8. #9	653-0197-58	Opelation connector ass'y	1
#10	653-0198-92	PH connector ass'y	1

■WIRE CONNECTION:


DSP(1) PWB
DSP(2) PWB
MAIN PWB
OPERATION(1) PWB
OPERATION(2) PWB
L.C.D
BACK LIGHT
DC-DC CONVERTER
BACK UP
GROUND
TO POWER AMP
AMP CONTROL
D/A CONTROL
YEL
BLK
BLU/WHT
PNK/WHT
FUSE (2A)
FROT/LEFT
FRONT/RIGHT
REAR/LEFT
REAR/RIGHT
R
L
RED
WHT

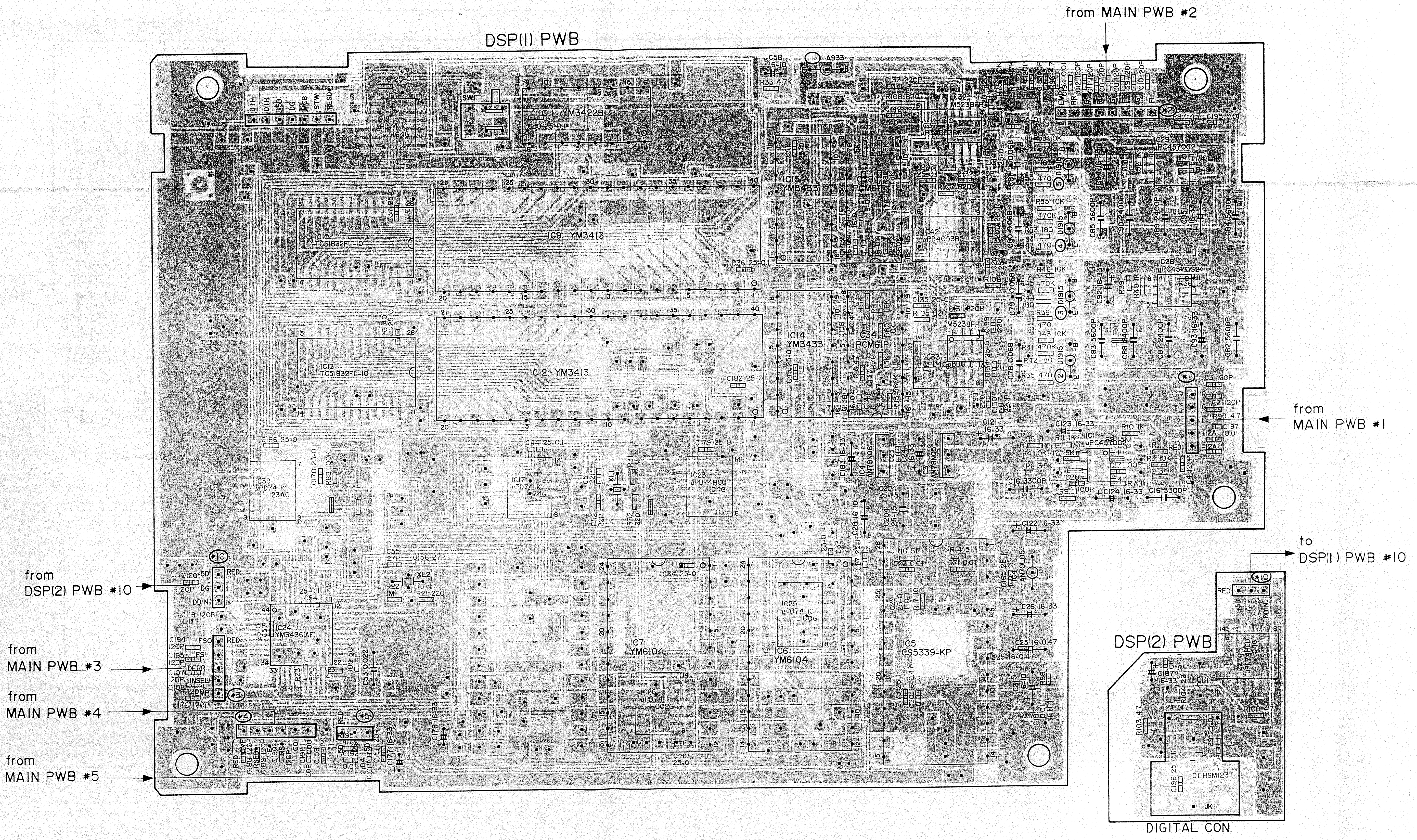
■PRINTED WIRING BOARD:

◉Main P.W.B section


MAIN PWB
to DSP(1) PWB #3
to DSP(1) PWB #4
from OPERATION(2) PWB #9
from OPERATION(1) PWB #6
to DSP(1) PWB #5
from FL TUBE
to DSP(1) PWB #1
to DSP(1) PWB #2
from OPERATION(2) PWB #8
to OPERATION(1) PWB #7
INVERTER UNIT
CN2
GRY
WHT
RED
BLK
L WHT
R RED
IC313 μPD27C512
IC316 TC5564APL-15
IC309 LC7535
IC308 LC7535
IC303 μPC812G
IC302 μPC812G
IC307 M5238FP
IC305 M5238FP
IC315 M6202IL
IC301 μPC4570
IC604 M53776A
IC611 μPC1093J
IC326 NJM79L05A
IC327 μPD74HC02G
IC312 XH032A0
IC322 μPD74HC00G
IC317 μPD74HC166G
IC325 μPD74HC02G
IC323 μPD74HC00G
IC318 μPD74HC273G
IC324 μPD74HC04G
K1095
D609 HRP32
D610 31D004
D601 P52I
D604 P52I
D653 1S1885
VR601
L601
L602
L603
L604
F601
CB302
CB301
CB303
R379 4.7K×8
R375 4.7K×8
R378 4.7K×8
R357 4.7K×4
R431 100K×4
X301
DATA
LCLK
CEA
CEC
CEB
INH
EMD
RR
G
RL
FR
FL
RESET
BLK

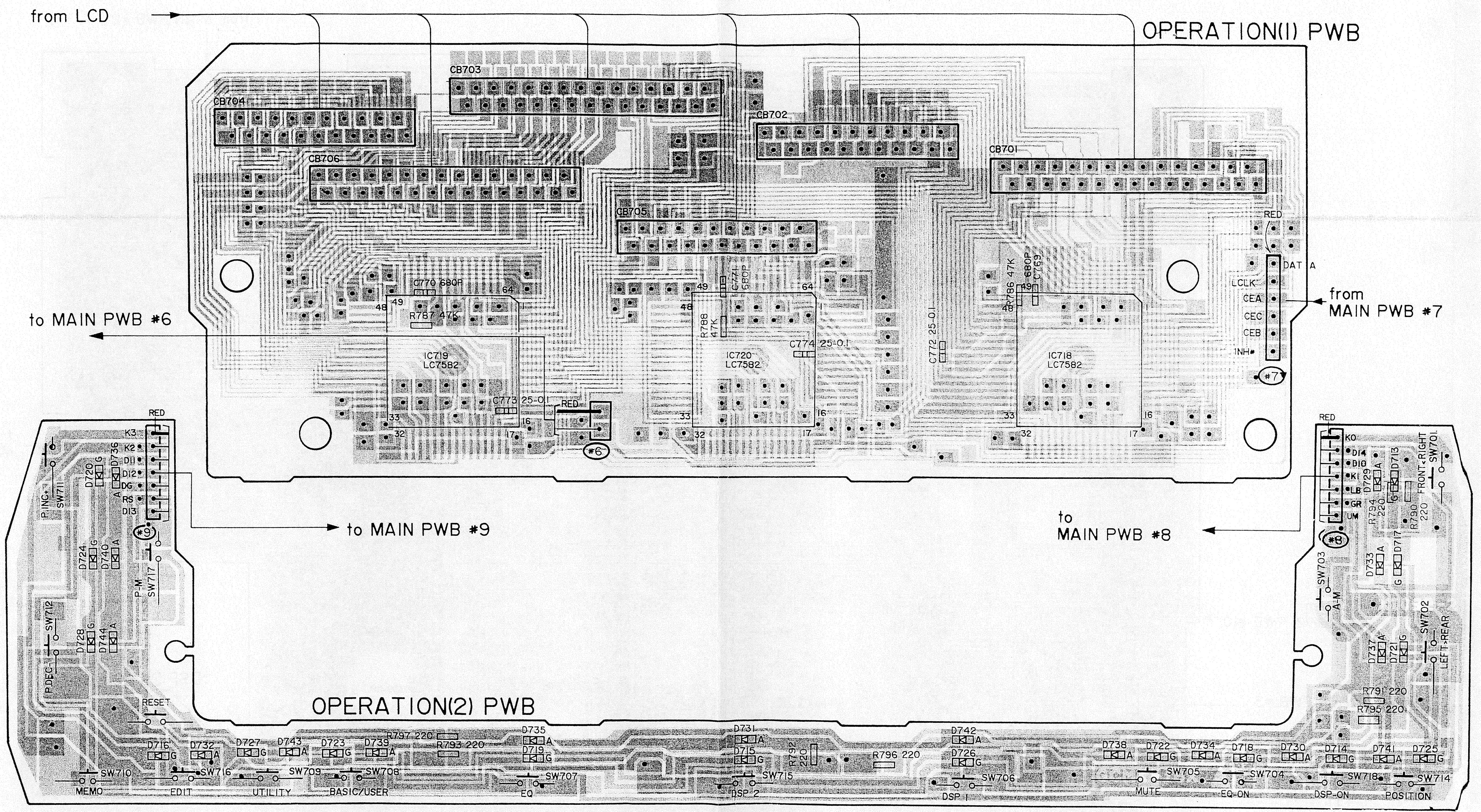
■PRINTED WIRING BOARD:

◉DSP P. W. B section


DSP(I) PWB
from MAIN PWB #2
from MAIN PWB #1
to DSP(I) PWB #10
from DSP(2) PWB #10
from MAIN PWB #3
from MAIN PWB #4
from MAIN PWB #5
DSP(2) PWB
DIGITAL CON.
IC9 YM3413
IC12 YM3413
IC10 TC51832FL-10
IC13 TC51832FL-10
IC11 YM3422B
IC15 YM3433
IC14 YM3433
IC33 PCM61P
IC34 PCM61P
IC7 YM6104
IC6 YM6104
IC5 CS5339-KP
IC24 YM3436(AF)
IC39 μPD74HC123AG
IC17 μPD74HC74G
IC23 μPD74HCU04G
IC25 μPD74HC00G
IC26 μPD74HC02G
IC19 μPD74HC164G
IC29 μPC4570G2
IC28 μPC4570G2
IC1 μPC4570G2
IC4 AN79N05
IC3 AN78N05
IC32 M5238FP
IC42 μPD4053BG
D1 HSM123
JK1
SW1
XL1
XL2

■PRINTED WIRING BOARD:

◉ Operation PWB



from LCD
OPERATION(1) PWB
CB704
CB703
CB702
CB706
CB701
CB705
C770 680P
R787 47K
IC719
LC7582
C773 25-0.1
RED
#6
to MAIN PWB #6
R788 47K
C771 680P
IC720
LC7582
C774 25-0.1
C772 25-0.1
R786 47K
680P
C769
IC718
LC7582
RED
DAT A
LCLK
CEA
CEC
CEB
INH
#7
from MAIN PWB #7
RED
K3
K2
DI1
DI2
DG
RS
DI3
#9
to MAIN PWB #9
to MAIN PWB #8
RED
K0
DI4
DI0
K1
LB
GR
UM
#8
P.INC+ SW711
D720
D736
D724
D740
P-M SW717
SW712
P.DEC-
D728
D744
RESET
OPERATION(2) PWB
D716
D732
D727
D743
D723
D739
R797 220
R793 220
D735
D719
D731
D715
R792 220
R796 220
D742
D726
D738
D722
D734
D718
D730
D714
D741
D725
SW710 MEMO
SW716 EDIT
SW709 UTILITY
SW708 BASIC/USER
SW707 EQ
SW715 DSP 2
SW706 DSP 1
SW705 MUTE
SW704 EQ-ON
SW718 DSP-ON
SW714 POSITION
FRONT/RIGHT SW701
D729
D713
R794 220
R790 220
D717
D733
SW703 A-M
SW702 LEFT/REAR
D737
D721
R791 220
R795 220

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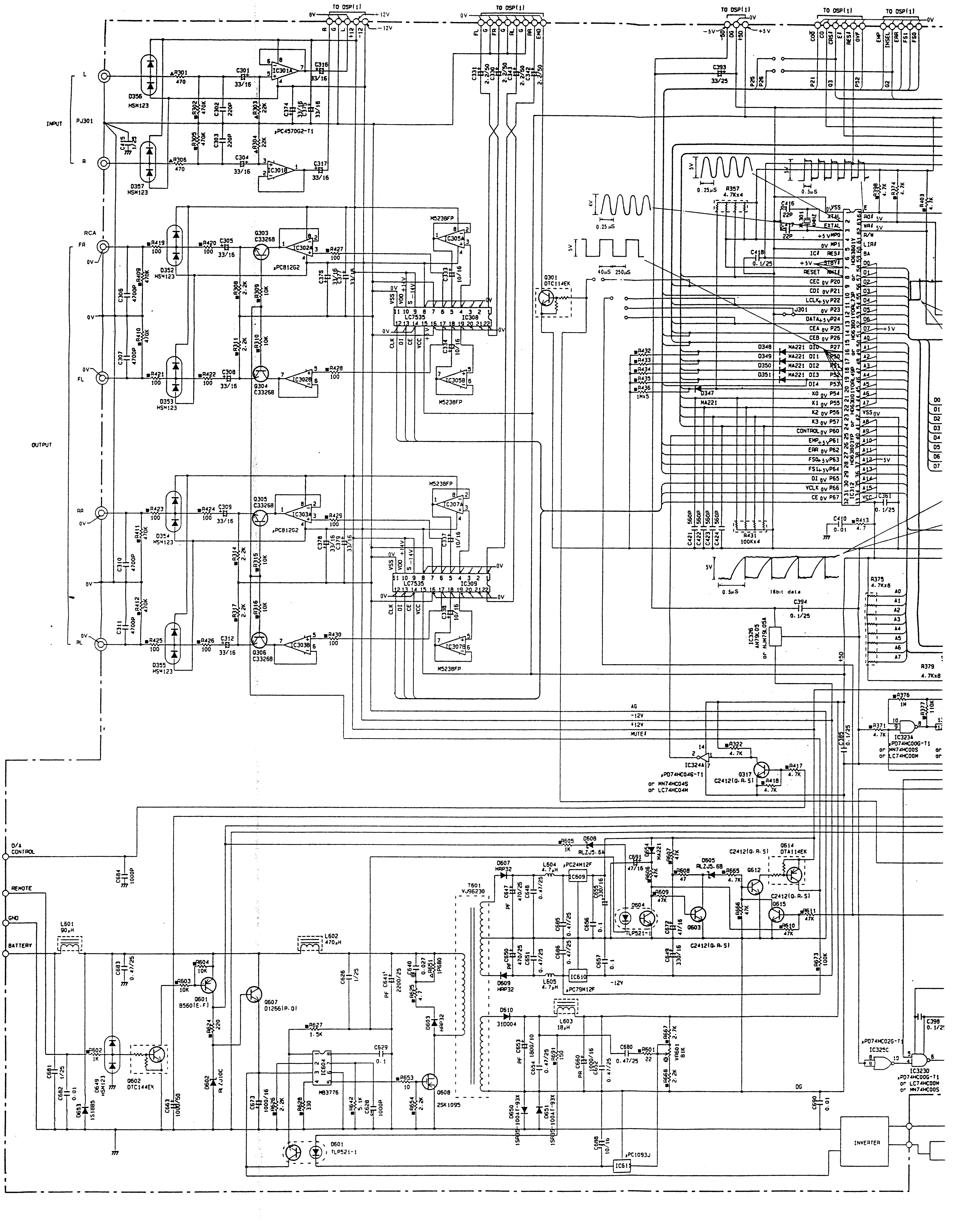
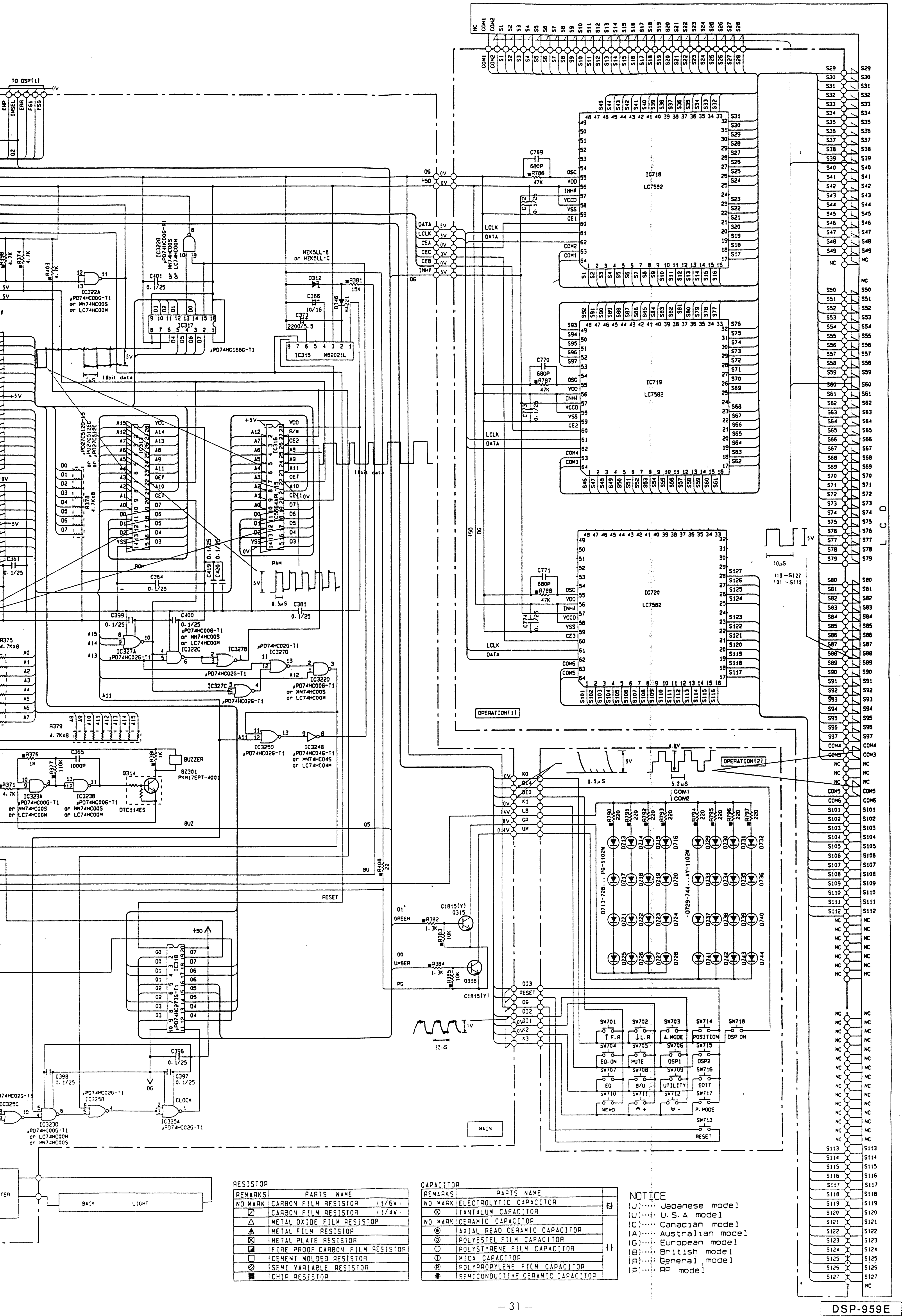
■CIRCUIT DIAGRAM: 1/2



TO DSP(1)
0V
+12V
-12V
+5V
-5V
INPUT
PJ301
L
R
RCA
FR
FL
RR
RL
OUTPUT
D/A CONTROL
REMOTE
GND
BATTERY
IC301A
IC301B
μPC4570G2-T1
D356
D357
HSM123
R301 470
R306 470
C301 33/16
C304 33/16
C316 33/16
C317 33/16
R302 470K
R305 470K
C302 220P
C303 220P
R303 22K
R304 22K
C415 1/25
Q303 C3326B
Q304 C3326B
Q305 C3326B
Q306 C3326B
IC302A
IC302B
IC303A
IC303B
μPC812G2
M5238FP
IC305A
IC305B
IC307A
IC307B
LC7535
IC308
IC309
VSS
VDD
CLK
DI
CE
VCC
D352
D353
D354
D355
C306 4700P
C307 4700P
C310 4700P
C311 4700P
R409 470K
R410 470K
R411 470K
R412 470K
Q301 DTC114EK
C393 33/25
P25
P26
P21
Q3
P52
Q2
CDO
CO
CRSI
EF
RESI
OVF
EMP
INSEL
ERR
FS1
FS0
R357 4.7K×4
C416 22P
C417 22P
X301 4MHz
C418 0.1/25
0.25μS
0.5μS
40μS
250μS
16bit data
J301
D348
D349
D350
D351
MA221
D347
R432
R433
R434
R435
R436 1M×5
HD63801Y
HD63801Y0AL73P
HD63801Y0AL49P
HD63803YP
IC312
C421 560P
C422 560P
C423 560P
C424 560P
R431 100K×4
C410 0.01
R413 4.7
C361 0.1/25
C394 0.1/25
IC326 AN79L05 or NJM79L05A
R375 4.7K×8
R379 4.7K×8
A0
A1
A2
A3
A4
A5
A6
A7
D0
D1
D2
D3
D4
D5
D6
D7
AG
MUTE
IC324A μPD74HC04G-T1 or MN74HC04S or LC74HC04M
R322 4.7K
Q317 C2412(Q.R.S)
R417 4.7K
R418 4.7K
C395 0.1/25
R376 1M
R377 110K
R371 4.7K
IC323A μPD74HC00G-T1 or MN74HC00S or LC74HC00M
C684 1000P
L601 90μH
L602 470μH
C683 0.47/25
C681 1/25
C682 0.01
D653 1S1885
D649 HSM123
R602 1K
Q602 DTC144EK
R603 10K
R604 10K
Q601 B560(E.F)
R624 220
Q607 D1266(P.Q)
D602 RL/J10C
C663 1000/50
T601 VJ96230
C626 1/25
C641 2200/25
C640 0.027
R651 1P680
R625 4.7
D603 HRP32
R627 1.5K
IC604 MB3776
C629 0.1
R653 10
Q608 2SK1095
C673 1000/16
R626 2.2K
R628 330
R642 5.1K
C628 1000P
R654 2.2K
D601 TLP521-1
D607 HRP32
L604 4.7μH
μPC24M12F
IC609
C647 470/25
C648 0.47/25
C655 330/16
C685 0.47/25
C656 0.1
C650 470/25
C651 0.47/25
C686 0.47/25
C657 0.1
D609 HRP32
L605 4.7μH
IC610
μPC79M12F
R605 1K
D608 RLZJ5.6A
C691 47/16
D604 TLP521-1
D654 MA221
R606 47K
R607 47K
R608 47
D605 RLZJ5.6B
R609 47K
C672 47/16
Q603
C2412(Q.R.S)
R665 4.7K
Q612
Q614 DTA114EK
R666 47K
Q615
R611 47K
R610 47K
C649 330/16
R673 100K
D610 31DQ04
L603 18μH
C653 1800/10
C654 0.47/25
R691 150
C660 1000/16
C652 0.47/25
C680 0.47/25
R601 22
R667 2.7K
VR601 81K
R668 2.2K
D650 1SR35-100AT-93X
D651 1SR35-100AT-93X
C698 10/16
μPC1093J
IC651
DG
C690 0.01
INVERTER
C398 0.1/25
μPD74HC02G-T1
IC325C
IC323D μPD74HC00G-T1 or LC74HC00M or MN74HC00S


TO DSP(1)
EMP
INSEL
EAR
FS1
FS0
IC718
LC7582
IC719
LC7582
IC720
LC7582
C769 680P
R786 47K
C770 680P
R787 47K
C771 680P
R788 47K
C772 0.1/25
C773 0.1/25
C774 0.1/25
OSC
VDD
INH#
VCCD
VSS
CE1
CE2
CE3
LCLK
DATA
COM1
COM2
COM3
COM4
COM5
COM6
DATA
LCLK
CEA
CEC
CEB
INH#
HZK5LL-B or HZK5LL-C
D312
R381 15K
C366 10/16
C373 2200/5.5
D346 MA121
IC315 M62021L
IC322A μPD74HC00G-T1 or MN74HC00S or LC74HC00M
IC322B μPD74HC00G-T1 or MN74HC00S or LC74HC00M
IC317 μPD74HC166G-T1
C401 0.1/25
18bit data
1μS
IC316 LC5564APL-15
RAM
μPD27C512D-15 μPD27C512EC or μPD27C512C
R378 4.7K×8
C361 0.1/25
C364 0.1/25
C419 0.1/25
C420 0.1/25
C381 0.1/25
C399 0.1/25
C400 0.1/25
0.5μS
R375 4.7K×8
IC327A μPD74HC02G-T1
IC322C μPD74HC00G-T1 or MN74HC00S or LC74HC00M
IC327B
IC327D μPD74HC02G-T1
IC322D μPD74HC00G-T1 or MN74HC00S or LC74HC00M
IC327C μPD74HC02G-T1
R379 4.7K×8
IC325D μPD74HC02G-T1
IC324B μPD74HC04G-T1 or MN74HC04S or LC74HC04M
R376 1M
C365 1000P
R377 110K
R380 1K
BUZZER
BZ301 PKM17EPT-4001
R371 4.7K
IC323A μPD74HC00G-T1 or MN74HC00S or LC74HC00M
IC323B μPD74HC00G-T1 or MN74HC00S or LC74HC00M
Q314
DTC114ES
BUZ
RESET
R408 22
Q1 GREEN
R382 1.3K
R383 10K
Q315 C1815(Y)
Q0 UMBER
R384 1.3K
R385 10K
Q316 C1815(Y)
PG
IC318 μPD74HC273G-T1
C396 0.1/25
C398 0.1/25
C397 0.1/25
CLOCK
IC325C μPD74HC02G-T1
IC323D μPD74HC00G-T1 or LC74HC00M or MN74HC00S
IC325B μPD74HC02G-T1
IC325A μPD74HC02G-T1
BACK LIGHT
OPERATION(1)
OPERATION(2)
0.5μS
5.2μS
4.8V
R790–R797 220
D713–D744
D713–728…PG-1102W
D729–744…AY-1102W
SW701 F.R
SW702 L.R
SW703 A.MODE
SW714 POSITION
SW718 DSP ON
SW704 EQ.ON
SW705 MUTE
SW706 DSP1
SW715 DSP2
SW707 EQ
SW708 B/U
SW709 UTILITY
SW716 EDIT
SW710 MEMO
SW711 ▲+
SW712 ▼-
SW717 P.MODE
SW713 RESET
MAIN
32μS
10μS
113~S127
101~S112
L C D

RESISTOR

REMARKS	PARTS NAME
NO MARK	CARBON FILM RESISTOR (1/5W)
▨	CARBON FILM RESISTOR (1/4W)
△	METAL OXIDE FILM RESISTOR
▲	METAL FILM RESISTOR
⊠	METAL PLATE RESISTOR
◪	FIRE PROOF CARBON FILM RESISTOR
□	CEMENT MOLDED RESISTOR
⊘	SEMI VARIABLE RESISTOR
■	CHIP RESISTOR

CAPACITOR

REMARKS	PARTS NAME
NO MARK	ELECTROLYTIC CAPACITOR
⊗	TANTALUM CAPACITOR
NO MARK	CERAMIC CAPACITOR
◉	AXIAL READ CERAMIC CAPACITOR
◎	POLYESTEL FILM CAPACITOR
○	POLYSTYRENE FILM CAPACITOR
⦶	MICA CAPACITOR
ⓟ	POLYPROPYLENE FILM CAPACITOR
✱	SEMICONDUCTIVE CERAMIC CAPACITOR

NOTICE
(J)····· Japanese model
(U)····· U.S.A model
(C)····· Canadian model
(A)····· Australian model
(G)····· European model
(B)····· British model
(R)····· General model
(P)····· RP model

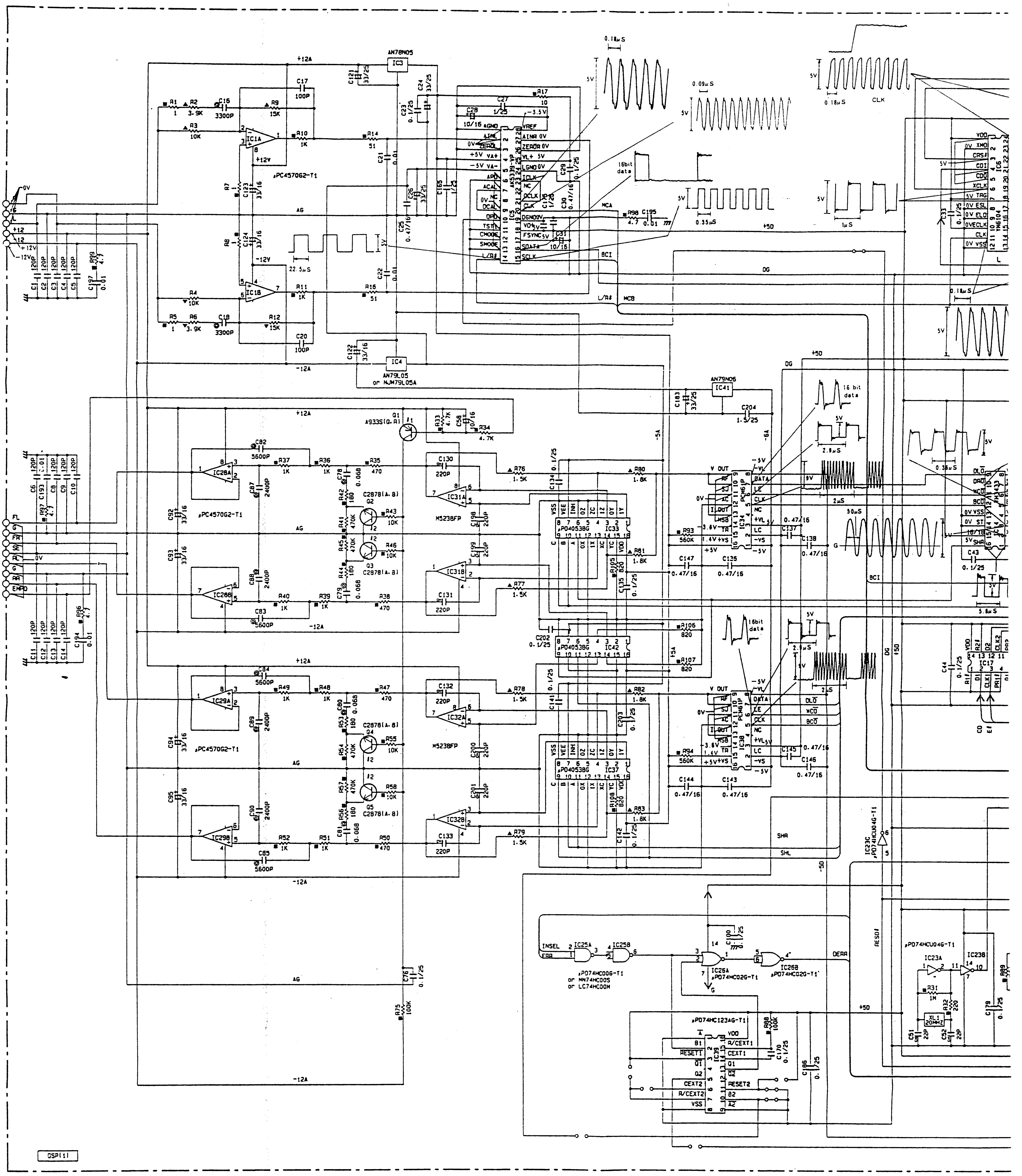
MAIN
POWER SUPPL

	LAST N
C	424 691
R	436 691
Q	317 515
D	357 654
IC	327 511

OPERATION

	LAST N
C	774
R	797
Q	
D	744
IC	720

■CIRCUIT DIAGRAM: 2/2


AN78N05
IC3
IC4
AN79L05
or NJM79L05A
AN79N06
IC41
IC1A
IC1B
μPC4570G2-T1
IC5
AK5339-VP
IC28A
IC28B
IC29A
IC29B
IC31A
IC31B
IC32A
IC32B
M5238FP
IC33
IC42
IC37
μPD4053BG
IC34
IC38
PCM61P
Q1
A933S(Q, R)
Q2
Q3
Q4
Q5
C2878(A, B)
IC25A
IC25B
μPD74HC00G-T1
or MN74HC00S
or LC74HC00M
IC26A
IC26B
μPD74HC02G-T1
IC39
μPD74HC123AG-T1
IC23A
IC23B
IC23C
μPD74HCU04G-T1
X1
20MHz
IC17
IC6
IO MAIN
+12A
-12A
AG
DG
+5D
-5D
-5A
16bit data
CLK
DSP(1)

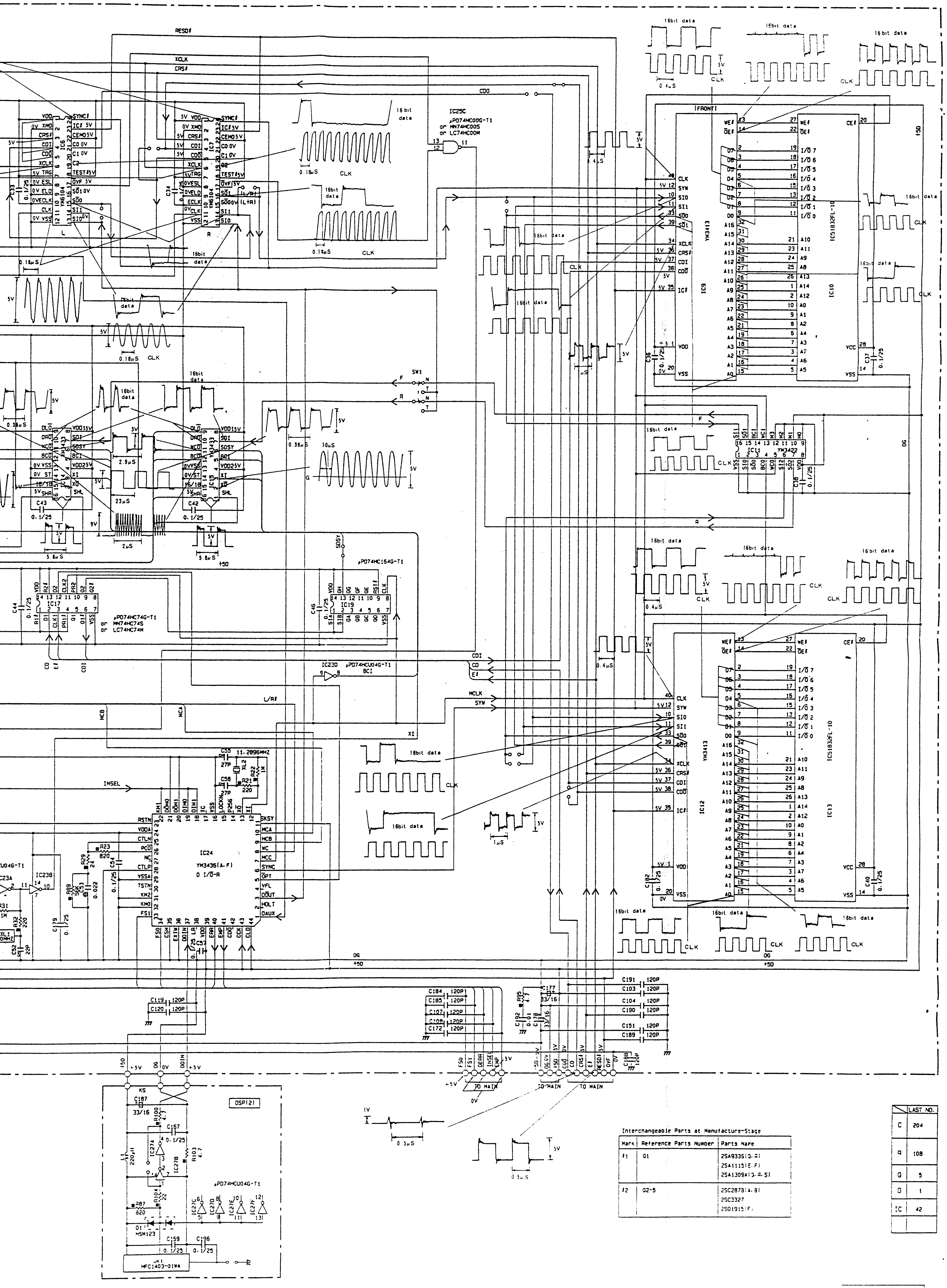
RESISTOR

REMARKS	PARTS NAME
NO MARK	CARBON FILM RESISTOR (1/6W)
⍁	CARBON FILM RESISTOR (1/4W)
△	METAL OXIDE FILM RESISTOR
▲	METAL FILM RESISTOR
⊠	METAL PLATE RESISTOR
▣	FIRE PROOF CARBON FILM RESISTOR
□	CEMENT MOLDED RESISTOR
⊘	SEMI VARIABLE RESISTOR
▬	CHIP RESISTOR

CAPACITOR

REMARKS	PARTS NAME	
NO MARK	ELECTROLYTIC CAPACITOR	⌗
⊗	TANTALUM CAPACITOR	
NO MARK	CERAMIC CAPACITOR	⊣⊢
◉	AXIAL READ CERAMIC CAPACITOR	
◎	POLYESTEL FILM CAPACITOR	
○	POLYSTYRENE FILM CAPACITOR	
⦶	MICA CAPACITOR	
Ⓟ	POLYPROPYLENE FILM CAPACITOR	
●	SEMICONDUCTIVE CERAMIC CAPACITOR	

NOTICE
(J)····· Japanese model
(U)····· U.S.A model
(C)····· Canadian model
(A)····· Australian model
(G)····· European model
(B)····· British model
(R)····· General model
(P)····· RP model


RESO#
XCLK
CRS#
CDO
IC25C
μPD74HC00G-T1
or MN74HC00S
or LC74HC00M
16bit data
CLK
0.18μS
IC6
YM6104
IC7
YM6104
IC9
YM3413
IC10
TC51832FL-10
IC12
YM3413
IC13
TC51832FL-10
IC14
YM3422
IC17
μPD74HC74G-T1
or MN74HC74S
or LC74HC74M
IC19
μPD74HC164G-T1
IC23D
μPD74HCU04G-T1
IC24
YM3435(A.F)
O I/O-A
11.2896MHZ
SW1
INSEL
L/R#
MCLK
SYW
MCB
MCA
XI
CDI
CO
E#
SOSY
(FRONT)
TO MAIN
DSP(2)
HSM123
HFC1403-01WA
μPD74HCU04G-T1
DG
+5D

Mark	Reference Parts Number	Parts Name
#1	Q1	2SA933S(Q.R) 2SA1115(E.F) 2SA1309A(Q.R.S)
#2	Q2-5	2SC2878(A.B) 2SC3327 2SD1915(F)

Interchangeable Parts at Manufacture-Stage

	LAST NO.
C	204
R	108
Q	5
D	1
IC	42